Non-ideal modelling and IMC based PID Controller Design of PWM DC-DC Buck Converter

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Abstract: This paper presents a non-ideal model of DC-DC PWM buck converter considering the parasitic elements (or non-idealities) such as equivalent series resistances (ESRs) of inductors and capacitors, parasitic resistances of semiconductor devices (diode, MOSFET) during conduction and the forward voltage drop of the diode. Incorporating this non-ideal model, a proficient PID control technique is proposed based on the internal model control (IMC) strategy. The salient features of proposed control methodology are: (i) tuning is such that the controller yields the desired bandwidth; (ii) unlike the conventional IMC-PID, the PID parameters are obtained by direct formula without trial and error. The proposed control scheme is simulated in MATLAB/SIMULINK and validated on a hardware setup using DSPACE DS1104 to confirm the superior results under variation of input voltage, reference voltage and load.

Keywords: Bandwidth, Buck converter, Internal model control, Non-ideal model, PID.

1. INTRODUCTION

Switched mode DC-DC power converters are very attractive, since its wide range of applicability in energy conversion, distribution generation and integration of renewable energy sources into the DC grid (Hossain and Rahim (2018)). Depending on the applications, various DC-DC converters have been utilized to step up/down the regulated DC voltage from the unregulated DC voltage. In practice, buck and synchronous buck converters are the most commonly used step down DC-DC converters (Erickson and Maksimovic (2007)).

In order to design accurate controller, modeling should be done precisely. In literature (Erickson and Maksimovic (2007); Middlebrook and Cuk (1976); Luo and Ye (2005); Garg et al. (2016)), many modeling techniques are presented, but the state space averaging (SSA) technique is the most popular. In all these, most of the time modeling has been done by considering the ideal behaviour of the elements. To the best of author's knowledge, no work is carried out for the modeling by considering all parasitic elements. Therefore in the present work, in order to obtain the accurate model, all parasitic resistances of elements are considered.

In literature, many control techniques based on sliding mode (Martinez-Salamero et al. (2010)), neural, fuzzy (Gupta et al. (1997)), model predictive (Geyer et al. (2008)), H-infinity Ioannidis and Manias (1999) etc., are reported for DC-DC converters. Despite the fact that, these control methods works fairly under various conditions, they incorporate heavy computation, tedious analysis and are tough to implement practically. On the contrary, many industrial applications prefer conventional PID controller theory due to its simple structure and low cost implementation (Garg et al. (2015)). In PID controller, the tuning parameters are calculated using trial and error method that requires considerable time to design and may sometimes fail to improve the performance. In order to overcome this, many PID tuning algorithms such as Zeigler-Nicholas (Z-N) (Skogestad (2003)), stability boundary locus (SBL) (Tan et al. (2006)), IMC (Rivera et al. (1986); Wei et al. (2009)) and various evolutionary tuning methods are reported. But there are limitations in using these; for example, Z-N technique can only give range of tuning values, SBL method provides region of stabilizing PI parameters, evolutionary techniques require some assumptions and involves complex iterative analysis. However, in comparison to other methods, IMC based PID tuning is model based, simple, robust and sub-optimal technique which requires only a single tuning parameter. It is observed that this tuning parameter is generally evaluated on the basis of trial and error method or approximation of plants time constants or optimizing some desired parameters (such as integral square error) or solving nonlinear equation with constraints on gain and phase margins, maximum sensitivity, etc (Laughlin et al. (1986)). This is the motivation for present work to tune single IMC parameter without using trial and error approach.

In this paper, the non-ideal model of DC-DC PWM buck converter is shown in section 2. Then the IMC based PID

design and a new approach to tune single IMC parameter in terms of desired gain crossover frequency is shown in section 3. Further, the proposed scheme is examined through simulations and experimental results in section 4. Finally, conclusions are drawn in section 5.

2. MODELING OF NON-IDEAL DC-DC BUCK CONVERTER

In this section, we present the non-ideal modeling of DC-DC PWM buck converter. The schematic representation is shown in Fig. 1. The circuit consists of switch (S), diode (D_d), inductor (L), capacitor (C) and load resistance (R). For obtaining nearly accurate model of buck converter, all parasitic resistances are considered such as source resistance (r_g), inductor resistance (r_L), switch resistance (r_{on}), diode resistance (r_d), diode forward voltage drop (v_{fd}), capacitor ESR (r_c). Further, V_g is input supply, v_o is output voltage, v_c is voltage across capacitor, v_L is voltage across inductor, D is duty cycle.

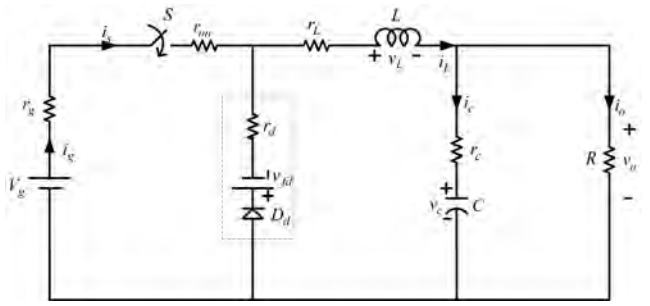


Fig. 1. Schematic of non-ideal DC-DC buck converter

2.1 During Switch On

When switch is ON (S_1), the equations governing with inductor current (i_L), capacitor voltage (v_c) and output voltage (v_o) are obtained as:

$$\frac{di_L(t)}{dt} = \left(-\frac{r_g + r_{on} + r_L}{L} - \frac{Rr_c}{L(R+r_c)}\right) i_L(t) + \left(-\frac{1}{L} + \frac{r_c}{(R+r_c)L}\right) v_c(t) + \frac{1}{L} v_g(t) \quad (1)$$

$$\frac{dv_c(t)}{dt} = \left(\frac{R}{C(R+r_c)}\right) i_L(t) - \left(\frac{1}{C(R+r_c)}\right) v_c(t) \quad (2)$$

$$v_o(t) = \left(\frac{Rr_c}{R+r_c}\right) i_L(t) + \left(\frac{R}{R+r_c}\right) v_c(t) \quad (3)$$

By using state space averaging (SSA) technique, (1), (2) and (3) can be written as

$$S_1 : \begin{cases} \dot{x}(t) = A_1 x(t) + B_1 u(t) \\ y(t) = C_1 x(t) \end{cases} \quad (4)$$

where, $x(t) = [\, i_L(t)\ v_C(t)\,]^T$, $u(t) = V_g$, $y(t) = [\, v_0(t)\ i_g(t)\,]^T$ and

2.2 During Switch OFF

When switch is OFF (S_0), the equations governing with inductor current (i_L), capacitor voltage (v_c) and output voltage (v_o) are determined as:

$$\frac{di_L(t)}{dt} = \left(-\frac{r_L + r_d}{L} - \frac{Rr_c}{L(R+r_c)}\right) i_L(t) + \left(-\frac{1}{L} + \frac{r_c}{L(R+r_c)}\right) v_c(t) - \frac{v_{fd}}{L} \quad (5)$$

$$\frac{dv_c(t)}{dt} = \left(\frac{R}{C(R+r_c)}\right) i_L(t) - \left(\frac{1}{C(R+r_c)}\right) v_c(t) \quad (6)$$

$$v_o(t) = \left(\frac{Rr_c}{R+r_c}\right) i_L(t) + \left(\frac{R}{R+r_c}\right) v_c(t) \quad (7)$$

By using state space averaging (SSA) technique, (5), (6) and (7) can be written as

$$S_0 : \begin{cases} \dot{x}(t) = A_2 x(t) + B_2 u(t) \\ y(t) = C_2 x(t) \end{cases} \quad (8)$$

From the small signal analysis of the buck converter, the transfer function associated with duty cycle to output voltage is given by,

$$G(s) = \frac{\tilde{v}_0}{\tilde{d}}(s) = C(sI - A)^{-1} B_d \quad (9)$$

where,

$$A = \begin{bmatrix} r_L + \frac{Rr_c}{R+r_c} + & -\frac{R}{L(R+r_c)} \\ -\frac{D(r_g + r_{on}) + D' r_d}{L} & \\ \frac{R}{C(R+r_c)} & -\frac{1}{C(R+r_c)} \end{bmatrix}$$

$$B_d = \begin{bmatrix} \frac{(-r_{on} - r_g + r_d) I_L + V_g + V_{fd}}{L} \\ 0 \end{bmatrix}$$

$$C = \begin{bmatrix} \frac{Rr_c}{R+r_c} & \frac{R}{R+r_c} \\ D & 0 \end{bmatrix} \quad (10)$$

Note 1: Here, $\tilde{v}_o$ and $\tilde{d}$ denote the small signal variations of output voltage and duty cycle.

Note 2: Without the loss of generality, for small signal analysis, $A = DA_1 + (1-D)A_2, B_d = (A_1 - A_2)X + (B_1 - B_2)U$ and $C = DC_1 + (1-D)C_2$.

Equation (9) can be further written as

$$G(s) = K \frac{n_1 s + n_0}{d_2 s^2 + d_1 s + d_0} \quad (11)$$

where,

$$K = \frac{V_g \left(1 + \frac{r_L + r_d}{R}\right) + V_{fd}\left(1 + \frac{r_L + r_g + r_{on}}{R}\right)}{\left[1 + \frac{r_L + D(r_g + r_{on}) + D' r_d}{R}\right]^2}$$

$$n_1 = Cr_c$$

$$n_0 = d_0 = 1$$

$$d_2 = \frac{LC\,(R + r_c)}{r_L + R + D\,(r_g + r_{on}) + D' r_d}$$

$$d_1 = \frac{L}{r_L + R + D(r_g + r_{on}) + D' r_d} + \frac{CR(r_L + D(r_g + r_{on}) + D' r_d)}{r_L + R + D(r_g + r_{on}) + D' r_d} + Cr_C$$

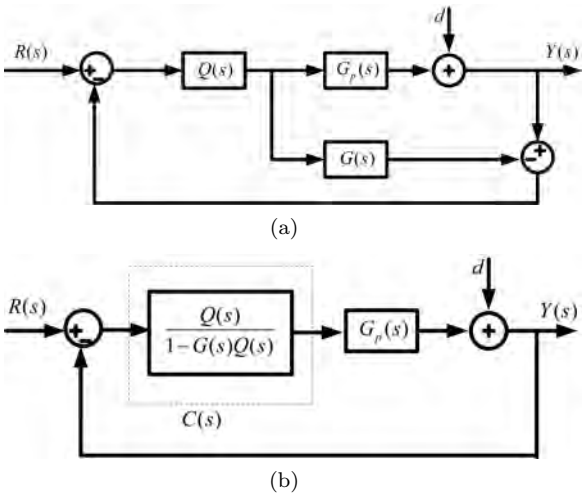


Fig. 2. (a) General IMC structure (Rivera et al. (1986))(b) Conventional control scheme

Note 3: When all the non-idealities are zero (*i.e.*, r_g=r_L=0, r_{on}=r_d=r_c=0, v_{fd}=0), then ideal transfer function can be obtained:

$$G_i(s) = V_g \frac{\frac{1}{LC}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}} \tag{12}$$

On substituting the values of elements from Table I in (11), (12) and by conducting time & frequancy response analysis, it is observed that the non-ideal model behaviour is very close to the practical model (*i.e.,* Hardware set-up).

3. PROPOSED CONTROLLER DESIGN

In this section, the IMC based controller for the model (11) of the DC-DC buck converter is proposed. The controller takes the form of PID cascaded with a lag term and its tuning is carried out on the basis of desired gain crossover frequency.

3.1 Controller Formulation

In IMC scheme, the controller encapsulates the plant model. In other words if the exact model of the plant to be controlled is known, then the perfect control is achieved. The IMC based control structure is shown in Fig. 2(a) (Rivera et al. (1986)), which can be further reconfigured into conventional feedback structure as shown in Fig. 2(b). The IMC-PID design procedure is given below.
Consider a stable proper finite dimensional plant as

$$G(s) = K\frac{N(s)}{D(s)} \tag{13}$$

where, $K > 0$, $N(s) = \sum_{i=0}^{n} n_i s^i$, $n_i > 0$, $D(s) = \sum_{i=0}^{n+1} d_i s^i$, $d_i > 0$. Using filter $F(s) = 1/f(s)$, where, $f(s) = (\lambda s + 1)^n$, $n \in N$, $\lambda > 0$, the IMC controller, $Q(s)$ is given by

$$Q(s) = \frac{1}{K}\frac{D(s)}{N(s)}F(s) \tag{14}$$

*Note 4:*A low-pass filter $F(s)$ is generally added in the control scheme to attenuate the effects of model mismatching.

Now, the IMC controller in (14) can be converted to the conventional feedback controller using synthesis equation

$$C(s) = \frac{Q(s)}{1 - G(s)Q(s)} \tag{15}$$

which yields

$$C(s) = \frac{1}{K}\frac{D(s)}{N(s)\left(f(s) - 1\right)} \tag{16}$$

With the aforementioned procedure, we design the controller for a second-order system (as the non-ideal model of buck converter is the second-order system with one left half plane (LHP) zero) as shown in (11), where,

$$N(s) = n_1 s + n_0 \tag{17}$$

$$D(s) = d_2 s^2 + d_1 s + d_0 \tag{18}$$

For a second-order system, generally a second-order filter is employed but here the first-order filter as suggested in (Saxena and Hote (2017)) is used to prevent excessive differential control action, *i.e.*,

$$f(s) = \lambda s + 1 \tag{19}$$

substituting (17), (18) and (19) in (16), we get,

$$C(s) = \left(k_p + \frac{k_i}{s} + k_d s\right)\frac{1}{N(s)} \tag{20}$$

where,

$$k_p = \frac{d_1}{K\lambda}, k_i = \frac{d_0}{K\lambda}, k_d = \frac{d_2}{K\lambda} \tag{21}$$

Note 5: Equation (20) states that, $C(s)$ acquires PID form followed by a lag term $\frac{1}{N(s)}$.

On substituting d_0, d_1 and d_2 from (11) in (21), we get tuning constants in terms of buck converter parameters as:

$$k_p = \frac{\left[\frac{L + Cr_c}{R} + C\left(r_L + D\left(r_g + r_{on}\right) + D^{'}r_d\right)\right]}{\left(1 + \frac{r_c}{R}\right)\left[1 + \frac{r_L + D\left(r_g + r_{on}\right) + D^{'}r_d}{R}\right]}}{\lambda\left[V_g\left(1 + \frac{r_L + r_d}{R}\right) + V_{df}\left(1 + \frac{r_L + r_g + r_{on}}{R}\right)\right]} \tag{22}$$

$$k_i = \frac{\left(1 + \frac{r_L}{R} + D\left(\frac{r_g}{R} + \frac{r_{on}}{R}\right) + D'\left(\frac{r_d}{R}\right)\right)^2}{\lambda\left(V_g\left(1 + \frac{r_L}{R} + \frac{r_d}{R}\right) + V_{fd}\left(1 + \frac{r_L}{R} + \frac{r_g}{R} + \frac{r_{on}}{R}\right)\right)} \tag{23}$$

$$k_d = \frac{LC}{\lambda}\frac{\left[1 + \frac{r_c}{R}\right]\left[1 + \frac{r_L + D(r_g + r_{on}) + D^{'}r_d}{R}\right]}{\left[V_g\left(1 + \frac{r_L + r_d}{R}\right) + V_{df}\left(1 + \frac{r_L + r_g + r_{on}}{R}\right)\right]} \tag{24}$$

Note 6: In case of ideal transfer function, the tuning constants (k_{po}, k_{io}, k_{do}) as follows:

$$k_{po} = \frac{L}{\lambda R V_g},\ k_{io} = \frac{1}{\lambda V_g},\ k_{do} = \frac{LC}{\lambda V_g}$$

3.2 λ Tuning

From the previous subsection, the controller is formulated which consists of only one parameter, *i.e.*, λ. In order to get the desired performance, we now present the tuning strategy. This tuning principle follows the concept of Bode's ideal transfer function. Consider an integrating type system in a feed forward path in classical control loop with gain k as

$$L(s) = C(s)P(s) = \frac{k}{s} \tag{25}$$

then the gain crossover frequency (ω_{gc}) becomes

$$\omega_{gc} = k \tag{26}$$

and phase margin $\phi = \pi/2$. It means that, ω_{gc} varies with k, however ϕ is insensitive to k. Now, the closed-loop system is given by

$$T(s) = \frac{L(s)}{1 + L(s)} = \frac{1}{1 + \frac{s}{k}} \tag{27}$$

Thus, the system exhibits infinite gain margin with the constant phase margin. Also, the unit step response of the closed-loop system (27) has the expression: $y(t) = 1 - e^{-kt} < 1,\ \forall k > 0,\ t > 0$ which does not exhibit overshoot. Hence, the overall relative stability of the system is improved.

Lemma 1 (Saxena and Hote (2017)): The closed loop transfer function of controlled system is equivalent to IMC filter when plant and model are same and controller is designed via IMC scheme.

Therefore using aforementioned lemma, we can state that the closed-loop transfer function is equivalent to the filter. So, it can be treated as a reference model as given in (27), *i.e.*,

$$T(s) = F(s) = \frac{1}{1 + \lambda s} \tag{28}$$

where $\lambda = \frac{1}{k}$. Now from (26), the gain crossover frequency is given by

$$\omega_{gc} = \frac{1}{\lambda} \tag{29}$$

Now consider the plant (13), whose numerator and denominator are described in (17) and (18), respectively. If $C(s)$ be a controller designed from IMC based controller, then $T(s)$ becomes

$$T(s) = \frac{G(s)C(s)}{1 + G(s)C(s)} \tag{30}$$

By substituting (13) and (16) in (30), we get the same result as in (28). Thus, the IMC controller for the non-ideal DC-DC buck converter system can be designed for desired gain crossover frequency.

Note 7: The gain crossover frequency should be in the range of one sixth to one tenth of switching frequency (Erickson and Maksimovic (2007)).

Table 1. Parameters of Buck Converter

Parameters	Value
Input voltage (V_g)	12V-15V
Source resistance (r_g)	0.03 Ω
Inductor (L/r_L)	489 μH/ 0.24Ω
Capacitor (C/r_C)	100 μF/ 0.1Ω
Diode forward drop (V_{fd})	0.5V
Diode resistance (r_d)	0.03 Ω
Switch resistance (r_{on})	0.05 Ω
Switching frequency (f)	20KHz
Load resistance (R)	10 Ω-20 Ω

Fig. 3. Experimental set-up

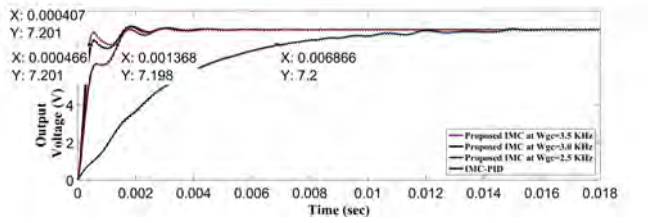


Fig. 4. Simulation results of transient response

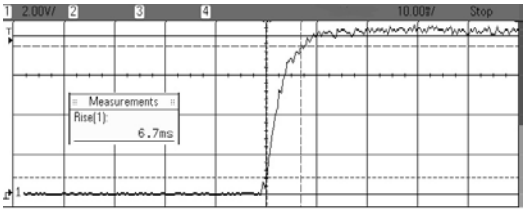
4. SIMULATION AND EXPERIMENTAL RESULTS

In this section, the proposed scheme is applied to the buck converter to observe the efficiency and advantages through simulations and hardware implementations. Table I shows the parameters of DC-DC buck converter for the current study.

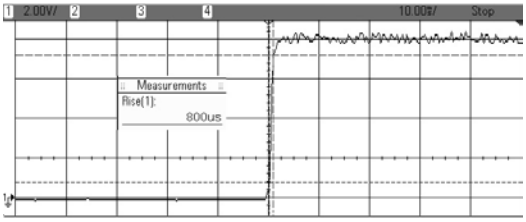
4.1 Controller Implementation

The schematic diagram and prototype of DC-DC buck converter set up are shown in Fig. 3. The proposed IMC and IMC-PID controllers are implemented by using DSPACE DS1104 digital controller board. The simulation parameters as well as hardware component specifications used for the prototype are given in Table I. The proposed PID controller parameters are $k_p = 1816$, $k_i = 2.086 \times 10^7$ and $k_d = 1$ for $\lambda = 2500$. The conventional IMC-PID parameters are evaluated as $k_p = 0.0024$, $k_i = 27.778$ and $k_d = 1.3 \times 10^{-6}$ for $\lambda = 0.0031$ which is obtained by trial and error method. The validation of controller performance is observed from transient response of the overall system and with three different conditions such as sudden changes in input and reference voltages and load.

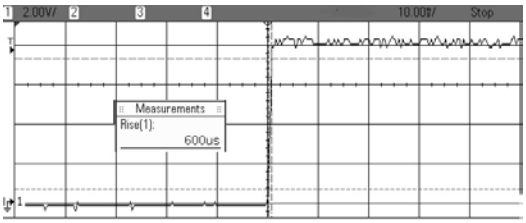
Transient Comparison The transient response of the complete system observed from simulation and hardware results are shown in Fig. 4 and Fig. 5, respectively. The performance of the proposed controller is also observed at different crossover frequencies. Almost similar behavior



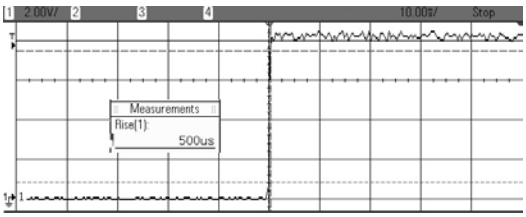
(a)



(b)



(c)



(d)

Fig. 5. Experimental result of transient response with (a) IMC-PID controller and proposed controller at (b) $\omega_{gc} = 2.5$ KHz, (c) $\omega_{gc} = 3$ KHz, and (d) $\omega_{gc} = 3.5$ KHz

Table 2. Rise time (s)

Method	ω_{gc}	Simulation	Experimental
IMC-PID	-	6800us	6700us
Proposed IMC-PID	2.5KHz	1200us	800us
	3.0KHz	466us	600us
	3.5KHz	407us	500us

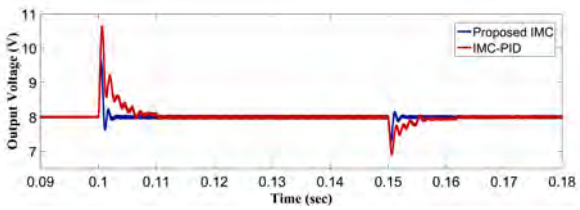
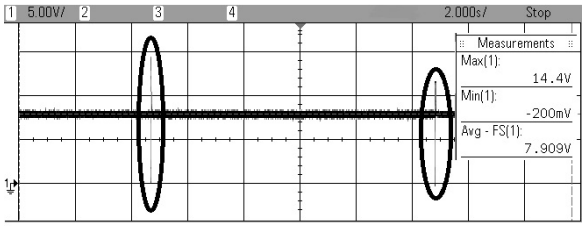
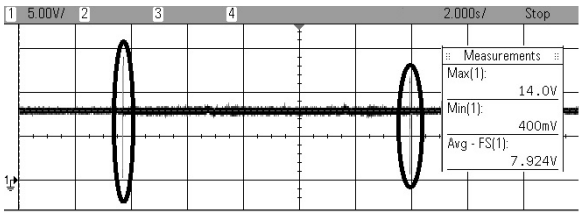


Fig. 6. Simulation results of sudden change in input voltage

is obtained in simulation and experimental results. From Table II, it is observed that the speed of response of the proposed controller is faster than that of the IMC-PID controller.



(a)



(b)

Fig. 7. Experimental results of output voltage for sudden change in input supply with (a) IMC-PID and (b) the proposed controller

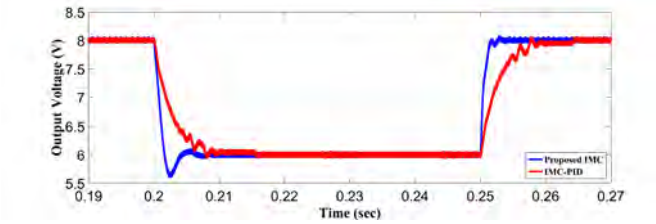
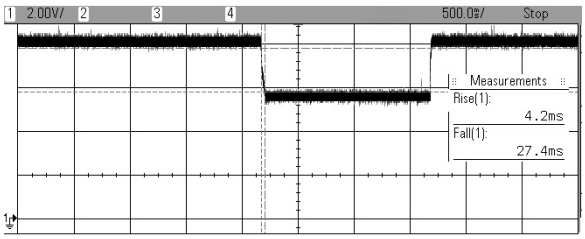
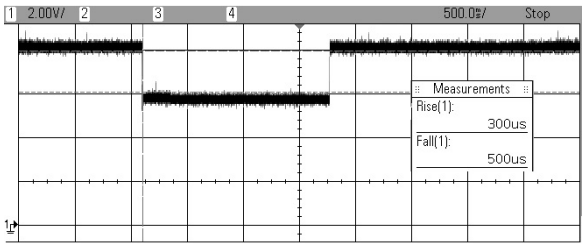


Fig. 8. Simulation results of sudden change in reference voltage



(a)



(b)

Fig. 9. Experimental results of output voltage for sudden change in reference voltage with (a) IMC-PID and (b) the proposed controller

Sudden Change in Input Voltage The overall system performance is monitored for sudden changes in input voltage while other all conditions are kept constant. At constant load $R = 10\Omega$, the input voltage is varied from $12V$ to $15V$ at $t = 0.1s$ and 15V to 12V at $t = 0.15s$. The corresponding simulation results with IMC-PID and

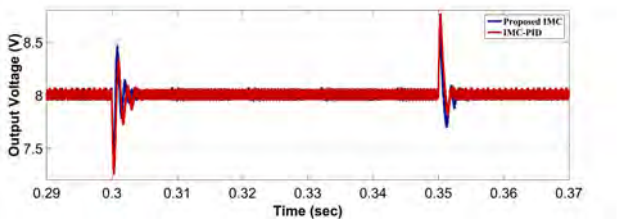


Fig. 10. Simulation results of sudden load change

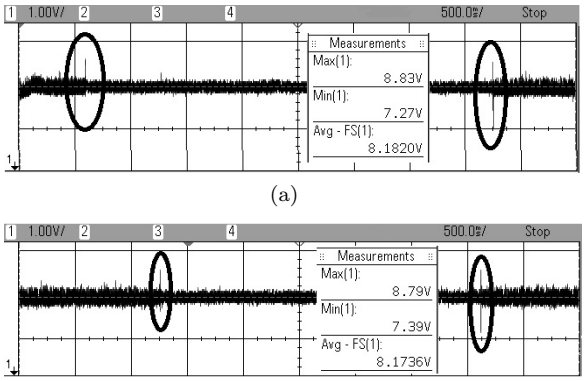


Fig. 11. Experimental results of output voltage for sudden change in load with (a) IMC-PID and (b) the proposed controller

proposed controller are shown in Fig. 6. To validate these simulation results, experimental results are also shown in Fig. 7.

Sudden Change in Reference Voltage The performance of the complete system for change in set point voltage, *i.e.*, output voltage, can be observed from the simulation and experimental results as shown in Fig. 8 and Fig. 9 respectively. As shown in Fig. 8, the reference voltage is changed from 8V to 6V at $t = 0.2s$ and 6V to 8V at $t = 0.25s$.

Sudden Load Change The overall system performance is monitored for sudden changes in load resistance while other all conditions are kept constant. The load resistance is changed from minimum (10Ω) to maximum (20Ω) and vice-versa at constant input voltage $V_g = 12V$. In this case, the load resistance is varied from 10Ω to 20Ω at $t = 0.31s$ and 20Ω to 10Ω at $t = 0.35s$. The corresponding simulation results with proposed controller and IMC-PID are shown in Fig. 10. To validate these simulation results, experimental results are shown in Fig. 11.

5. CONCLUSION

This work presents the non-ideal modelling of DC-DC buck converter and a voltage control scheme via IMC is proposed. The controller acquires a PID form and all the tuning parameters are explored on the basis of desired gain crossover frequency. The simulation and hardware experiment validates the quality of the designed controller. The proposed controller brings improved dynamic and steady state performance for buck type converters. In future, we will consider the more realistic model in which the parameter variation exists and the same proposed controller scheme will be applied to obtain the same functionality of the system. Further, this scheme will be extended to other (non-minimum phase) type of DC-DC converters.

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