A Class of Impedance Tomography based Sensors for Semiconductor Manufacturing

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Abstract— **This paper explores the feasibility of a class of sensors for semiconductor manufacturing based on Electrical Impedance Tomography. We briefly summarize the role of sensors in semiconductor manufacturing and the essential principles of Electrical Impedance Tomography. In this paper we discuss the design and operation of a prototype etch rate sensor based on these ideas. We also propose a novel sensor to measure the wafer potential during semiconductor manufacturing. We discuss simulation results from this novel sensor.**

Keywords

Electrical Impedance Tomography, modeling, estimation, sensors, semiconductor manufacturing.

I. INTRODUCTION

In this paper, we investigate the feasibility of a class of sensors for semiconductor manufacturing applications. These sensors are fully autonomous *vis-a-vis* power, communication, and transduction. They externally resemble standard silicon wafers, and can therefore be deployed without expensive equipment modifications and have access to the equipment and process during processing. The variables that these sensors can measure include etch rate, temperature, and plasma induced potentials. The common theme shared by this class of sensors is that they are based on Electrical Impedance Tomography (EIT). EIT is an *in vivo* imaging technology that has found widespread use in biomedical applications.

Djamdji *et al*. were the first to propose an EIT based measurement strategy for semiconductor manufacturing [4]. They used EIT to infer resistivity maps of various thin conductive films on wafers. Their experimental results show that EIT methods are applicable to a wide range of sheet resistance values with resolution, accuracy and repeatability comparable to traditional four point probe measurements. In this paper we investigate how EIT can be used to measure other variables of interest during semiconductor manufacturing. To our knowledge, the use of EIT in semiconductor manufacturing applications as suggested in this paper is novel.

Briefly, EIT involves injecting electrical currents into an object while measuring the induced potentials on the surface of the object. The internal conductivity distribution can be approximately deduced from these measurements. In a semiconductor manufacturing context, chemical and physical effects can induce conductivity changes in the interior of the wafer being processed. By placing electrodes at the wafer periphery and measuring potentials across these electrodes, we can infer conductivity changes. This can, in turn, be related to direct physical and chemical effects through process models. The main advantages of EIT based techniques are that they are cost-effective and non-invasive. We have built a prototype etch rate sensor based on this technology. In this paper, we discuss design details and results from experimental studies of this prototype sensor. We also introduce a novel EIT-based sensor to measure the induced potential at the wafer surface during plasma etching. This sensor utilizes a network of discrete transduction elements.

The remainder of this paper is organized as follows. A brief discussion of the role of sensors in semiconductor manufacturing is offered in Section 2. Following this, the general EIT problem is presented in Section 3. In Section 4 and 5 we discuss the design and operation of a prototype etch rate sensor based on EIT techniques. In Section 6 we propose an alternative approach to EIT based on a network of discrete, resistive transduction elements. In Section 7 we illustrate this approach with simulation results of a novel wafer potential sensor. Finally, we draw conclusions and discuss future research directions in Section 8.

II. SENSORS IN SEMICONDUCTOR MANUFACTURING

Recently, semiconductor manufacturing practice has evolved from using off-line to in-line metrology to monitor, diagnose, and control processes. In-line metrology allows every wafer to be inspected after processing. Processing tools have also been equipped with sensors to measure process variables and, where possible, wafer state information during processing (in-situ measurements). The benefits are numerous, including improved process monitoring, reduced product variance, higher throughput and the possibility of run-to-run control. However, the associated engineering and operating costs can be significant as the complexity of the processing tool increases. Processing tools become also more vulnerable to metrology errors and/or failure.

A promising alternative to in-line and/or in situ metrology is to use an autonomous sensor wafer. This is a sensor

that externally resembles a standard silicon wafer with embedded power, communications, and transduction elements. Such a sensor wafer can be introduced into equipment with existing wafer-handling robotics in cassette-to-cassette operations as a regular product wafer. It can access wafer and process state information during processing as is available from equipment-based in-situ sensors. In addition, sensor wafers can be significantly less expensive and complex when compared with in situ or in line alternatives.

The feasibility of on-wafer sensors for use during semiconductor processing has been shown in [7]. However, a large number of sensors have to be used to obtain reasonable spatial resolution across the wafer, particularly for 300 mm substrates. This makes the design, fabrication, and operation of these wafers increasingly complex. The sensor wafer must also resemble a regular product wafer as closely as possible in order to avoid interference of the sensor wafer with the variable to be measured. Thermal mass and local topology of the sensors should, therefore, be reduced to a minimum. Hence, best results will be obtained with sensor wafers which are fabricated with semiconductor compatible materials and processing techniques.

III. ELECTRICAL IMPEDANCE TOMOGRAPHY

Electrical Impedance Tomography is an in-vivo imaging technique, principally used in medical applications. This technique consists of injecting electrical currents into an object and measuring the induced potentials at the surface of the object. These surface measurements are used to estimate the conductivity distribution in the interior of the object. The estimated conductivity distribution can then be directly related to different features within the object and can, therefore, be used as a diagnostic tool. The principal advantage of this technique is that it uses fairly inexpensive hardware and is non-destructive.

Consider an object with conductivity $\sigma(\mathbf{r})$ as function of the spatial position $\mathbf{r}$ in the object. From Maxwell's equations one can then derive the following Laplacian-like partial differential equation for the electrical potential distribution u in the interior Ω of a body [2]:

$$\nabla \circ [\sigma(\mathbf{r})\nabla u] = 0, \text{ in } \Omega. \tag{1}$$

In the remainder we will assume that currents are injected through discrete electrodes at the periphery $\partial\Omega$ of the object, resulting in non-zero normal current densities J_k at each electrode:

$$\sigma\left(\nabla u \circ \hat{\mathbf{n}}\right)(\mathbf{r}) = \begin{cases} -J_k & \text{at } k\text{-th electrode} \\ 0 & \text{elsewhere} \end{cases}. \tag{2}$$

To avoid the accumulation of charge in the object during the experiment, we have to add the following constraint on this boundary condition:

$$\int_{\partial\Omega} \sigma\left(\nabla u \circ \hat{\mathbf{n}}\right)(\mathbf{r}) = 0.$$

The PDE in (1) together with the boundary condition in (2) yields a solution u that is unique upto an arbitrary additive constant. A unique solution can be obtained by assigning a ground potential to a point inside or on the boundary of the object. We will make this assignment so as to satisfy the constraint

$$\int_{\partial\Omega} u = 0.$$

For a given conductivity distribution $\sigma(\mathbf{r})$ inside the object and a known current density at the surface the continuum model, defined by (1) and (2), can be used to predict the potential inside the object. The *forward problem* is concerned with solving these equations for u. For simple geometries and conductivity distributions, we can find analytical solutions. However, for arbitrary conductivity distributions we must resort to numerical methods such as the Finite Element Method (FEM).

Consider the following experiment. Known currents are applied to electrodes on the surface of an object and the corresponding potentials on the electrodes are measured. The central question in EIT is then whether it will be possible to reconstruct $\sigma(\mathbf{r})$ based on these simple electrical measurements. This problem is called the *inverse problem* and is in general non-linear and poorly conditioned. It is poorly conditioned because large changes in conductivity in the center of the object weakly influence the measured potential at the boundary. In addition, measurement noise can seriously influence the final estimate.

In order to solve the inverse problem, the conductivity distribution inside the object is parameterized, yielding a modest number of unknown parameters. For example, some EIT algorithms assume that the object can be split up into N smaller elements, each with a constant conductivity $\sigma_i, i = 1, 2, \cdots, N$. With L electrodes on the boundary any EIT experiment will yield at most $L(L-1)/2$ independent measurements [2]. Consequently, the number of unknown parameters in the conductivity parameterization must be less than $L(L-1)/2$.

The inverse problem reduces to finding the optimal $\boldsymbol{\sigma}$ in the chosen parameterization such that the potentials on the electrodes in the forward model, $\mathbf{U}(\boldsymbol{\sigma})$, match the measured electrode potentials $\mathbf{V}$. An appropriate criterion would be to minimize the error according to a statistical criterion

$$\min_{\boldsymbol{\sigma}} E(\boldsymbol{\sigma}) = \min_{\boldsymbol{\sigma}} \|\mathbf{U}(\boldsymbol{\sigma}) - \mathbf{V}\|^2. \tag{3}$$

Differentiating the cost functional $E(\boldsymbol{\sigma})$ in (3) yields

$$g(\boldsymbol{\sigma}) = \nabla E(\boldsymbol{\sigma}) = \mathbf{J}^T\left(\mathbf{U}(\boldsymbol{\sigma}) - \mathbf{V}\right) \tag{4}$$

where $\mathbf{J} = \nabla \mathbf{U}(\boldsymbol{\sigma})$ is the Jacobian matrix. The optimal conductivity distribution, $\boldsymbol{\sigma}_{opt}$ satisfies $g(\boldsymbol{\sigma}_{opt}) = 0$. However, $\boldsymbol{\sigma}_{opt}$ cannot be found analytically as $g(\boldsymbol{\sigma})$ in (4) is nonlinear. We therefore have to resort to nonlinear programming techniques to estimate $\boldsymbol{\sigma}_{opt}$. Here, assume that we have an initial estimate $\boldsymbol{\sigma}^{(n)}$ which is close to $\boldsymbol{\sigma}_{opt}$. In order to find an improved estimate $\boldsymbol{\sigma}^{(n+1)}$ of $\boldsymbol{\sigma}_{opt}$ we expand $g(\boldsymbol{\sigma})$ in (4) as a Taylor series around $\boldsymbol{\sigma}^{(n)}$, i.e.

$$g(\boldsymbol{\sigma}^{(n+1)}) = g(\boldsymbol{\sigma}^{(n)}) + g'(\boldsymbol{\sigma}^{(n)})\Delta\boldsymbol{\sigma} + \text{h.o.t.} \tag{5}$$

where $\Delta\boldsymbol{\sigma} = \boldsymbol{\sigma}^{(n+1)} - \boldsymbol{\sigma}^{(n)}$ and $g'(\boldsymbol{\sigma}^{(n)}) \approx J^T J$. Setting (5) equal to zero and solving for $\Delta\boldsymbol{\sigma}$ finally results in the following iterative procedure [10]:

$$
\begin{aligned}
\Delta\boldsymbol{\sigma} &= -\left(\mathbf{J}^T\mathbf{J}\right)^{-1}\mathbf{J}^T\mathbf{V}_{\text{diff}} & (6)\\
\mathbf{V}_{\text{diff}} &= \mathbf{U}(\boldsymbol{\sigma}^{(n)}) - \mathbf{V}, & (7)\\
\boldsymbol{\sigma}^{(n+1)} &= \boldsymbol{\sigma}^{(n)} + \Delta\boldsymbol{\sigma}. & (8)
\end{aligned}
$$

In this iterative procedure the electrode potentials have to be computed for each updated conductivity distribution. Hence, an efficient implementation of the complete electrode model is essential.

IV. ETCH RATE SENSOR WAFER DESIGN

During semiconductor manufacturing, chemical and physical effects can induce conductivity changes in the interior of the wafer. Placing electrodes at the periphery of a wafer and measuring the potentials on these electrodes during semiconductor manufacturing allows us to infer these conductivity changes using the EIT algorithm (6) - (8). In turn, these changes in conductivity can be related to chemical and/or physical effects using appropriate models. Hence, it is possible to design a class of simple sensors for semiconductor manufacturing based on EIT techniques. The small size of the electrodes, the placement of the electrodes at the periphery of the wafer, and the large number of independent degrees of freedom (32 electrodes results in at most 496 degrees of freedom to fit the conductivity profile to the observed data) make this class of sensors attractive for use during semiconductor manufacturing. Among the different chemical and physical effects which can be measured are temperature, etch rate, and plasma induced potentials. The geometry of the sensor (thickness of conductive layer $\ll$ diameter) justifies the assumption that the EIT problem is two dimensional (2D).

As proof-of-concept, we have developed a simple prototype etch rate sensor based on EIT for in-line and in-situ measurements during semiconductor manufacturing. This sensor exploits the fact that the conductivity σ of a thin conductive film is proportional to the thickness t of the film, i.e. $\sigma = t/\rho$ where ρ is the resistivity of the film material. Assuming that ρ does not change during processing, a change in the conductivity distribution of the wafer during processing can provide valuable spatial etch rate information.

The sensor wafer is fabricated using simple semiconductor processing techniques. A standard 4 inch wafer is first oxidized to create an electrically isolated substrate. A conductive layer of doped poly-silicon is then deposited onto the substrate. A patterning step defines a circular disk (radius = 3.5 cm) in the conductive poly-Si layer. After aluminum deposition, a second patterning step defines 16 or 32 evenly spaced electrodes at the edge of the poly-Si disk. Aluminum leads connect the electrodes to an array of contact pads on the wafer. A photograph of the finished wafer is shown in Figure 1.
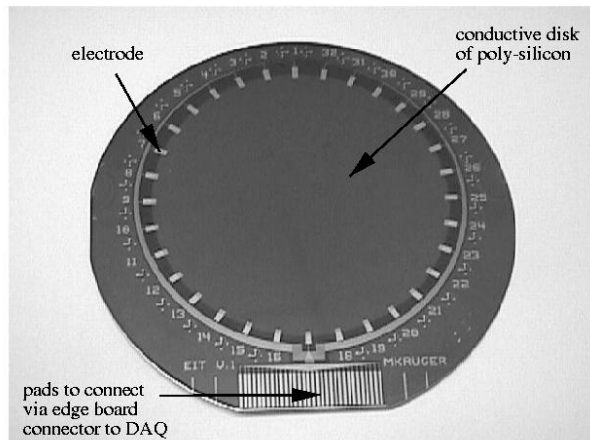

Fig. 1. Picture of prototype etch rate sensor.

An edge board connector is used to connect the electrodes via the contact pads on the wafer to a data acquisition (DAQ) system. The DAQ system can select any two electrodes through which a current enters and leaves the conductive disk. For each current pattern, the resulting potential on each electrode is measured. In order to reduce the noise on the data, the electrode potentials are averaged over multiple samples.

To test the prototype etch rate sensor, etch experiments were performed in the Berkeley Microfabrication lab. The experiments consisted of several etching cycles. After each cycle, the wafer was connected to the DAQ system with the edge board connector. DC currents were injected between opposite electrodes and the resulting DC electrode potentials (averaged over 100 samples) were recorded and stored for off-line analysis.

V. ETCH RATE RESULTS

The sensor wafer in this experiment consisted of 16 equally spaced electrodes around a poly-Si disk with radius $r = 3.5$cm. The poly-Si layer was lightly doped with an average thickness $t = 2144$Å and an average sheet resistance $R_s = 86.2$Ohm/$\square$. The sensing area was completely exposed to the etchant, allowing spatial etch rate measurements to be performed. All aluminum lines were covered with a thin layer of photoresist to prevent them from being attacked by the wet etchant.

The sensor wafer was subjected to five timed etching cycles (for a total of 165 seconds) by immersing it in a bath containing silicon etchant (50 HNO_3 : 20 H_2O : 1 NH_4F). To slow down the etch rate, the etchant was diluted with H_2O. After each etch cycle, the wafer was connected to the DAQ system and subjected to 50 EIT experiments, each consisting of 16 opposite current patterns. The resulting potentials at all electrodes were then recorded and stored for later analysis. In addition, the thickness of the poly-Si layer was optically recorded at 36 sites across the wafer.

The silicon etchant advances faster along the grain boundaries of the poly-Si layer, resulting in increased surface
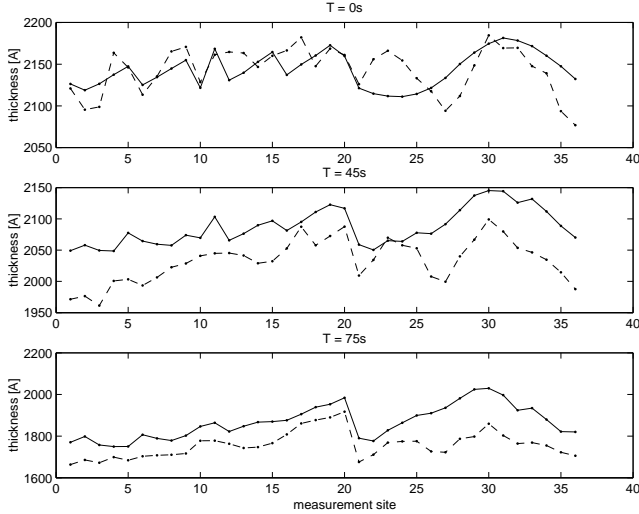
Fig. 2. Absolute thickness in Å after 0, 45 and 70 seconds of exposure to the etchant: optical measurements (solid) and EIT-sensor (dashed).

roughness over time. After the third etching cycle, the roughness caused unacceptable variance in the optical thickness measurements. Consequently, we were not able to validate the EIT experiments after the third etching cycle.

After each etching cycle, we applied the EIT algorithm (6) - (8) to the measured electrode potentials, averaged over the 50 EIT experiments, to estimate the absolute conductivity distribution across the sensor wafer. In our EIT algorithm, the conductivity distribution inside the sensor wafer was assumed to be a function of the conductivity at the 36 measurements sites. Ordinary kriging [8], [3] was then used to obtain an estimate of the conductivity distribution across the wafer.

Converting the estimated conductivity distribution σ to a thickness distribution t according to $t = \sigma\rho$ requires knowledge of the resistivity ρ of the poly-Si film. We used the value of ρ which minimizes the error between the optical thickness measurements and the EIT-based thickness estimates of the unetched film. The measured thickness at the 36 measurement sites after 0, 45 and 75 seconds of exposure to the etchant is shown in Figure 2. This graph clearly shows that there is no strong correlation between the optical thickness measurement and the EIT-based thickness measurement. The most likely factors, causing this discrepancy, are nonlinearities in the DAQ system, undermodeling of the electrodes and biases in the potential measurements. It is likely, though, that these factors remain constant over time, i.e. we can obtain unbiased differential measurements by simply subtracting the initial thickness measurements from subsequent thickness measurements. Differential thickness measurements at the 36 measurement sites after 45 and 75 seconds of exposure to the etchant are shown in Figure 3. The differential thickness measurements observed with the EIT sensor correlate well with the differential optical measurements. However, an increasing bias is clearly visible. This bias can be attributed to the fact that we are not measuring the same variable. The EIT based
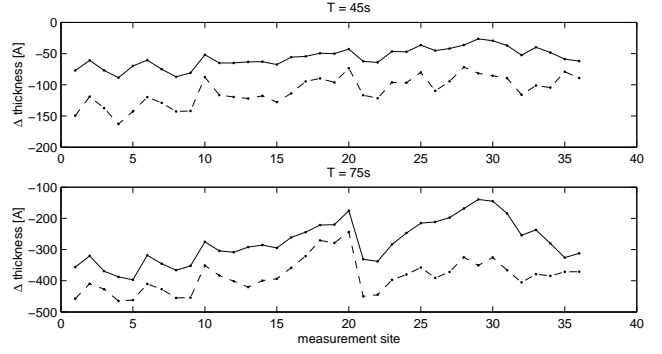

Fig. 3. Differential thickness in Å after 45 and 75 seconds of exposure to the etchant: optical measurements (solid) and EIT-sensor (dashed).
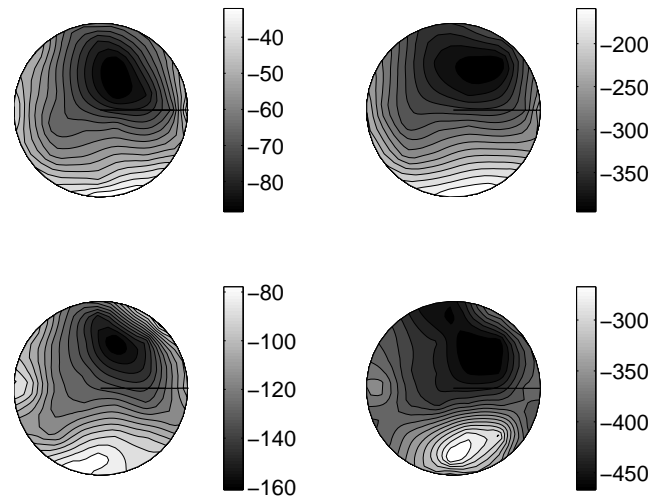

Fig. 4. Change in thickness in Å after 45s (left panels) and 75s (right panels); optical measurements (top panels), EIT sensor (bottom panels).

sensor measures *electrical* film thickness. During etching the etch front progresses faster along the grain boundaries of the poly-Si, causing surface roughness. Consequently, the electrical film thickness will be smaller than the optical film thickness. Over time, surface roughness increases, causing the bias between the two to increase as well.

In order to assess the spatial measurement capabilities of the prototype etch rate sensor we included differential thickness profiles across the wafer as measured optically as well as with the EIT-based sensor, see Figure 4. Both the optical metrology tool and the EIT-based sensor show the same remarkable etching pattern, corresponding to a rather nonuniform etch.

VI. EIT APPLIED TO A RESISTIVE NETWORK

Traditional EIT techniques have been successfully applied to a variety of applications, including our etch rate sensor. However, these traditional EIT approaches have several downsides. First, it can be very difficult to accurately model the object of interest including the electrode on its boundary. An inaccurate model in the forward problem results in erroneous predictions for the potentials on the periphery which, in turn, can yield erroneous conductivity

distributions in the inverse problem. Second, the iterative approaches utilized in many EIT algorithms are slow and computationally expensive. Many EIT algorithms rely on FEM techniques to solve the forward problem numerically. However, the accuracy and speed of these FEM techniques depends on the discretization used. A coarse discretization (i.e. relatively few nodes and elements) will speed up the computation. However this gain in speed comes at the expense of accuracy in the forward problem, which, in turn will affect the accuracy of the inverse problem. Finally, the sensitivity to changes in conductivity is not uniform across the object. For example, conductivity changes near the periphery are easier to detect than changes in the center. Consequently, small amounts of noise on the potential measurements can significantly affect the estimated conductivity profile.

In stark contrast with traditional EIT applications, in the semiconductor metrology context we have the luxury of designing the object being imaged. In this section we exploit this idea and offer a novel approach based on a resistive network with discrete transduction elements. Note that this approach was inspired by work performed by Baroudi *et al.* [1].

The FEM technique, utilized in many EIT algorithms to solve the forward problem, models the conductive continuum inside the object as a large resistive network. Hence, a natural step in our context is to replace the conductive continuum at the wafer surface with an array of discrete transduction elements to create a resistive network as shown in Figure 5. Such a resistive network can circumvent the following problems associated with traditional EIT approaches. First, the topology of the resistive network and the individual conductance of each transduction element can be designed to enhance the overall sensitivity, even in the remote interior of the object. Second, modeling a network of discrete resistive elements accurately is much simpler than modeling a conductive continuum. Finally, the number of transduction elements, and hence, the size and computational complexity of the resulting resistive network will be dictated by the number of independent measurements in the EIT experiment instead of the accuracy needed in the forward problem.

VII. Wafer potential sensor

A significant problem encountered in plasma etch processes during semiconductor manufacturing is the undesired accumulation of charge on dielectric materials at the wafer surface. This accumulation of charge can be particularly detrimental to the thin gate oxide in metal oxide semiconductor (MOS) devices, reducing device yield and reliability [5], [6]. Consequently, there is a need to measure and ultimately control wafer charging effects during semiconductor manufacturing.

In this section we conduct a feasibility study of a novel EIT-based sensor which measures charge accumulation at the wafer surface during plasma processing. The proposed
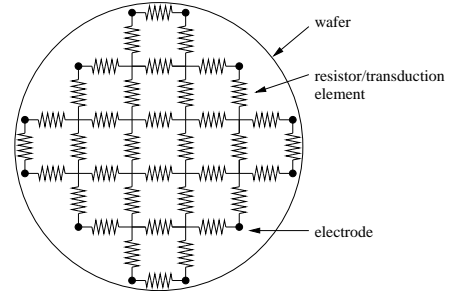

Fig. 5. Generic resistive network on wafer.

sensor employs discrete transduction elements whose conductivity is modulated by the magnitude of the electric field across a dielectric film at the wafer surface. A suitable device for this purpose is the depletion-mode N-type MOS Field Effect Transistor (NMOSFET) [9], a 4 terminal semiconductor device which can modulate the current flow between the source and drain terminals by applying an electric field between the gate and base terminals. This device conducts currents for positive as well as small negative gate potentials. During plasma processing the gate is exposed to the plasma, allowing positive or negative charges to accumulate. This, in turn, modulates the conductivity of the device.

To test the feasibility of a potential sensor based on a network of depletion mode NMOSFETs, we performed simulation studies on a simple network containing 6 of these devices (see Figure 6) in Hspice, an analog circuit simulator. This network contains 4 "electrodes", i.e. nodes through which currents can be injected into the network. This network was used to create *artificial* measurement data, which, in turn, was used to estimate the gate potential of each transistor in the network.

Each gate was assigned a potential between -2.5V and 2.5V. The network was then excited by different current patterns between pairs of electrodes. An iterative algorithm similar to (6) - (8) was developed to solve the inverse EIT problem for the network of transistors. In each iteration, the forward problem is solved in Hspice for the most recent estimate of the gate potentials. In addition, the Jacobian matrix is computed by perturbing each gate potential by a small percentage. The simulated electrode potentials are then compared to the artificial measurement data and the errors between them are used to update the estimate of the gate potentials. The simulation started with an initial guess of 0V for each gate potential. The gate potentials, as estimated by the algorithm, are shown in Figure 6. This graph clearly shows that the estimated gate potentials converge within 10 iterations to the real gate potentials.

VIII. Conclusions

In this paper we have explored the feasibility of a novel class of sensors for semiconductor manufacturing based on Electrical Impedance Tomography. We discussed the
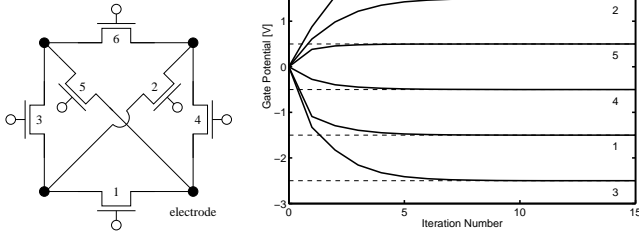
Fig. 6. Simulation results with resistive network of 6 depletion mode NMOSFETs.

design and operation of an etch rate sensor. In addition, we proposed a novel sensor which can measure the wafer potential during plasma processing. Unlike traditional EIT applications, this novel sensor employs a network of discrete resistive elements.

The simulation and experimental results presented in this paper show that the concept of EIT based sensors for use in semiconductor manufacturing is indeed feasible. Design and operation of EIT based sensors can be simple and cost-effective. The main challenge is in estimating the conductivity distribution in the interior of the sensor based on electrical measurements at the edge of the sensor. The estimated conductivity can then, in turn, be related to the variable of interest through chemical or physical models.

Therefore, we believe that the class of sensors, suggested in this paper, could someday provide a low cost alternative for in-situ spatial measurements across a wafer during semiconductor manufacturing. Future work will involve the implementation and characterization of the proposed wafer potential sensor.

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