Practical Techniques for Optimal Dual-Rate Digital Redesign

C.A. Rabbath, N. Lechevin and N. Hori

Abstract— **This paper proposes optimal dual-rate digital redesign methods that can be applied to continuous-time and fast-rate discrete-time control systems. Given a continuous-time control system, or a fast discrete-time control system, the paper presents techniques relying on the solution of a dual-rate H-2 discrete-time control problem to convert such systems to either a slow-rate or a dual-rate sampled-data control system while guaranteeing closed-loop stability and performance in the discrete-time H-2 sense. The proposed techniques result in sampled-data control systems having satisfactory performances over an extended range of sampling rates, when compared with other widely used methods of digital redesign. Furthermore, the proposed digital redesign techniques are useful in practice since they allow the designer to constrain the complexity of the digital controllers. Numerical examples demonstrate the performance of the proposed digital redesign techniques and provide a comparison with well-known approaches.**

I. INTRODUCTION

Digital controllers form integral parts of robotic and aerospace control systems, just to name a few, due to their relatively low cost, high reliability and flexibility, and compactness. To calculate the digital controllers, the method known as digital redesign has been proven effective in the past and been widely used in industry. Digital redesign is the process of converting a known continuous-time (CT) control system to a sampled-data (SD) control system. With digital redesign, the discrete-time (DT) controllers are obtained either by discretizing the individual CT controllers [1] or by using sophisticated methods that take into account the closed-loop topology and the plant dynamics [2]. Dual-rate digital redesign is defined in this paper as the conversion of a known CT control system, which satisfies the design specifications, to a dual-rate SD control system. A successful digital redesign results in a SD control system exhibiting closed-loop stability, a relatively close performance with that of the CT control system, and DT controller implementations free from numerical problems. Tools such as CT lifting [3] and DT lifting [4] may be involved in dual-rate digital redesign to facilitate the development. The idea of performing digital redesign and to obtain a dual-rate SD control system has been presented in works such as [2], [5], [6], [7]. Dual-rate control does not, by itself, prevent closed-loop instability that may arise when using relatively slow sampling. Closed-loop stability depends on the digital redesign method used along with the sampling periods selected for the implementation. The work in [2] has motivated the development of digital redesign taking into account the CT control system structure and the plant dynamics in order to provide satisfactory closed-loop performances for the SD control systems (such as closed-loop stability) at slow sampling periods for which classical, local digital redesign approaches [1] fail to do so. References [5] and [8] propose such techniques. The method of [5] uses two rates in the digital redesign process, whereas that of [8] uses a single rate. It should be pointed out that there exists a problem similar to that of digital redesign of a CT system; that is, the digital redesign of a fast DT system. Such digital redesign may be useful when the rate of a well-designed DT control system is too fast for practical implementation and one needs to redesign the fast DT control system to a slow DT control system while preserving closed-loop performance.

This paper proposes optimal dual-rate digital redesign methods that can be applied to CT and fast-rate DT control systems. Given a CT control system, or a fast DT control system, the paper presents techniques, which rely on the solution of a dual-rate H_2 DT control problem, to convert such systems to either a slow-rate or a dual-rate SD control system while guaranteeing closed-loop stability and performance in the DT H_2 sense. The idea of performing digital redesign using the H_2 method comes from [9], [10], although the authors have proposed methods that result in single-rate SD control systems. Here, the proposed dual-rate digital redesign techniques result in either single- or dual-rate SD control systems providing satisfactory closed-loop performances over an extended range of sampling rates, as compared with other widely used methods of digital redesign. Furthermore, the proposed dual-rate digital redesign techniques are very useful in practice since they allow the designer to constrain the complexity of the digital controllers. The proposed optimal dual-rate digital redesign methods are carried out in four consecutive steps: 1) Fast discretization of CT control system, 2) Dual-rate generalized plant modeling, 3) Solution to H_2 optimal dual-rate DT problem, and 4) DT controller order reduction. The methods of dual-rate digital redesign proposed in this paper apply to unstable, non-minimum phase CT plants as well as single- and multi-loop systems. The proposed dual-rate digital redesign techniques are, however, constrained by the specific requirements that arise when solving a DT H_2 problem.

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II. DUAL-RATE DIGITAL REDESIGN

A. ASSUMPTIONS & NOTATION

The following assumptions are assumed to hold unless explicitly stated otherwise.

Assumption 1: The systems are linear, SISO and have zero initial conditions.

Assumption 2: The CT control systems (or fast DT control systems) to be digitally redesigned have satisfactory performance characteristics, such as sufficient margins of stability, good transient and steady-state behaviors, appropriate disturbance rejection properties, and reasonable robustness.

Assumption 3: The uniform sampling periods used in the SD control systems are h (corresponding to slow rate of $1/h$ Hz) and T (corresponding to a fast rate of $1/T$ Hz). The periods are related as $h = N \cdot T$, $N \in \mathcal{Z}^+$, where $\mathcal{Z}^+$ is the set of positive integers. T is chosen to be non-pathological [10] with respect to the plant transfer function and the plant-input transfer function, which is the transfer function from the reference input to the plant input. As is well known, this does not cause any practical inconvenience.

Assumption 4: The hold device H and ideal sampler S, which can each take a period equal to T or h, are synchronized at time $t = 0$. The hold has a bounded response to a unit DT impulse input and does not introduce any discrete zero in the hold-equivalent model of the plant which cancels a pole of the plant model at non-pathological T values.

Assumption 5: The exogenous inputs to the control systems lie in the space $\mathcal{S}_c$; that is, the space of functions which have a finite supremum norm and are uniformly continuous over $[0, \infty)$, and independent of T.

In this paper, a DT signal with period p is expressed as $u(k, p)$, where the arguments are the time step $k \in \mathcal{Z} = \{\cdots, -2, -1, 0, 1, 2, \cdots\}$ and the sampling period p, which is T or h. The z-transform of $u(k, p)$ is given by $U(z, p)$, for either sampling period T or h; that is, for simplicity, z represents the complex variable in either case. For instance, the transfer function of a DT system G is given as $G(z, p)$.

B. PROPOSED METHODS

With the assumptions known, the steps of the proposed digital redesign methods are given as follows.

STEP 1: Fast discretization of CT control system.

The CT control system to be redesigned is shown in Figure 1(a). Let $\overline{G}$ have a realization $[\overline{A}_{\overline{G}}, \overline{B}_{\overline{G}}, \overline{C}_{\overline{G}}, \overline{D}_{\overline{G}}]$, where $\overline{A}_{\overline{G}} \in \mathcal{R}^{n\times n}$, $\overline{B}_{\overline{G}} \in \mathcal{R}^{n\times 1}$, $\overline{C}_{\overline{G}} \in \mathcal{R}^{1\times n}$, and $\overline{D}_{\overline{G}} \in \mathcal{R}$. $\mathcal{R}$ is the set of real numbers. The CT plant $\overline{G}(s)$ may comprise actuator and sensor dynamics. The hold-equivalent discretization of $\overline{G}$, at the fast rate of $1/T$, is performed as follows. Precede $\overline{G}(s)$ by a hold device H and place the ideal sampler S at the output of $\overline{G}(s)$. The resulting DT system $S\overline{G}H$ is then given as

$$\begin{aligned} x^{he}(k+1,T) &= e^{\overline{A}_{\overline{G}}T}x^{he}(k,T) \\ &\quad + \textstyle\int_{v=0}^{T} e^{\overline{A}_{\overline{G}}(T-v)}\overline{B}_{\overline{G}}dv \cdot u(k,T),\ x^{he}(0,T) = 0_{n\times 1}, \\ y^{he}(k,T) &= \overline{C}_{\overline{G}}x^{he}(k,T) + \overline{D}_{\overline{G}} \cdot u(k,T) \end{aligned} \tag{1}$$

where the superscript 'he' denotes hold equivalence and the fact the state and output of this system are different from those obtained with another discretization or from those of $\overline{G}(s)$ at the samples, $u(k, T)$ is the DT input to the zero-order hold (ZOH) which precedes the plant, $y^{he}(k, T)$ is the sampled plant output, and $k \in \mathcal{Z}$. The transfer function of $S\overline{G}H$ is given by $G(z, T)$. Proceed similarly for $\overline{A}(s)$, $\overline{B}(s)$ and $\overline{C}(s)$. Then, there results a fast, single-rate DT closed-loop system, as shown in Figure 1(b). The selection of T depends on the design specifications and on the dynamics of the system under control. Theorem 1 warrants closed-loop performance of the single-rate DT control system obtained by fast discretization of the CT control system.

Theorem 1 Consider the stable CT control system of Figure 1(a) and the closed-loop system of Figure 1(b), where H is the ZOH and S is the ideal sampler. Both control systems are subjected to exogenous inputs in $\mathcal{S}_c$. Then, the CT plant input and output of the control system of Figure 1(b) converge, uniformly-in-time, to those respective signals of the CT control system of Figure 1(a), as $T \to 0$, provided that the DT control system of Figure 1(b) internally stabilizes the plant at the T values selected.⋈
Proof: For brevity, the reader is referred to [11].□

Remarks 1) The convergence property expressed in Theorem 1 guarantees that there exists a (relatively short) T such that fast discretization results in satisfactory closed-loop performance. In other words, by making T short enough, the theorem provides conditions such that the tracking performance of the fast DT closed-loop system of Figure 1(b) is as close as desired to that of the CT control system of Figure 1(a). 2) When the closed-loop system to be redesigned is already a fast DT system, *step 1* should be ignored.

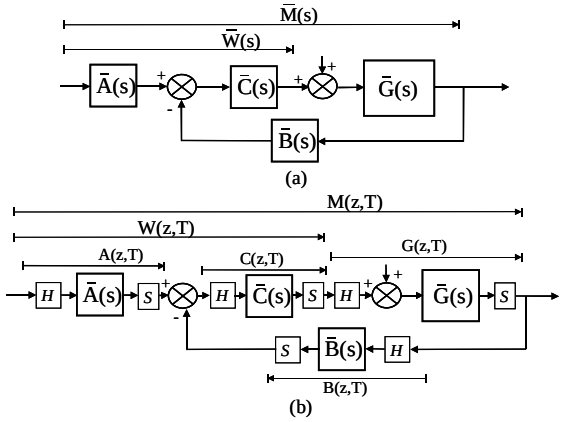

Figure 1: (a) CT control system and (b) control system obtained by fast discretization

STEP 2: Dual-rate generalized plant modeling.

With the knowledge of the DT controller transfer functions $A(z,T)$, $B(z,T)$, and $C(z,T)$, and of the DT plant $G(z,T)$, a generalized plant model can be constructed, as shown in Figure 2. The block diagram of Figure 2 is intended for step-tracking purposes. In the figure, the gain $\rho \in \mathcal{R}$ is a weight on the difference in plant input signals that can be tuned by the designer [9]. L represents the DT lifting operation and L^{-1} is the inverse DT lifting [4]. Note that $L^{-1}L = I$, so no information is lost when successively applying lifting and inverse lifting on a DT signal [10]. The generalized plant of Figure 2 is dual-rate due to the presence of $H_{h,T}$, $\widetilde{H}_{h,T}$, S_h and S_h^g. Systems $H_{h,T}$ and $\widetilde{H}_{h,T}$ are dual-rate generalized holds [12]. Such holds receive a DT input signal with period h (slow rate) and output a DT signal at period T (fast rate). System S_h is a DT system that takes a DT input signal at period T and outputs a DT signal having period h; that is, it decimates the input signal by a factor N. System S_h^g is a generalized dual-rate sampler which receives a DT input signal with period T and outputs a DT signal at period h. To understand the behavior of the generalized dual-rate sampler, consider $S_h^g L^{-1}$. The generalized dual-rate sampler used in Figure 2 is given by

$$y(k,h) = \begin{bmatrix} \frac{1}{N} & \cdots & \frac{1}{N} \end{bmatrix} \begin{bmatrix} u(Nk,T) \\ \vdots \\ u(Nk+N-1,T) \end{bmatrix}. \tag{2}$$

From (2), it can be seen that $S_h^g L^{-1}$ outputs an average value of the entries of the lifted N-vector input signal, at step kh. Corollary 1 provides a known limiting behavior for $S_h^g L^{-1}$ in connection with the fast-rate DT systems $W(z,T)$ and $M(z,T)$ shown in Figures 1(b) and 2.

Corollary 1 Given 1) the conditions of Theorem 1 are satisfied, 2) $H_{h,T}$ is the DT ZOH [12] and 3) H is the ZOH with period h, then the generalized sampler (2) is such that, for a fixed N, as the fast discretization $T \to 0$ (hence, as the lifting period $h \to 0$), the outputs of the closed-loop systems $HS_h^g M H_{h,T}$ and $HS_h^g W H_{h,T}$ converge uniformly-in-time to those of $\overline{M}$ and $\overline{W}$, respectively.⋈

Proof: Consider systems $HS_h^g M H_{h,T}$ and $\overline{M}$. The same development applies to systems $HS_h^g W H_{h,T}$ and $\overline{W}$. From the conditions of Theorem 1 and the presence of $H_{h,T}$ (the DT ZOH) and H (the ZOH), the output of $HS_h^g M H_{h,T}$ preserves the area under the output response curve that is obtained by placing a ZOH of period T at the output of $MH_{h,T}$, when subjected to a reference input in $\mathcal{S}_c$. With the same input to $MH_{h,T}$ and $\overline{M}$, it is clear that Theorem 1 is satisfied. Thus, by making T short enough (and hence h small), uniform-in-time convergence of the CT output of $HS_h^g M H_{h,T}$ to that of $\overline{M}$, for the same input in $\mathcal{S}_c$, is guaranteed.□

Remarks 1) Sampler S_h^g given by (2) provides information on the fast-rate DT system in the form of a DT scalar signal having period h. 2) With Corollary 1, the portions of the block diagram shown in Figure 2 corresponding to systems $S_h^g M H_{h,T}$ and $S_h^g W H_{h,T}$ are guaranteed to exhibit a known behavior as the periods T and h approach zero.

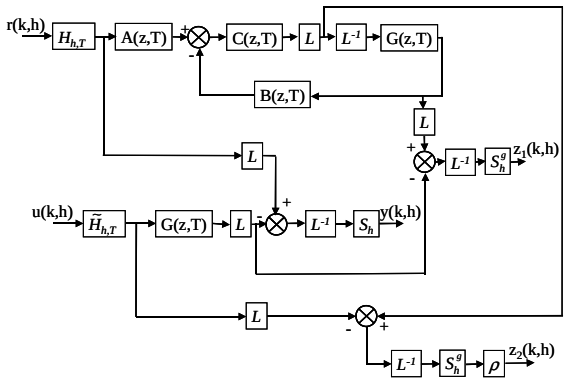

Figure 2: Dual-rate generalized plant $\widehat{G}(z,h)$

STEP 3: Solution to H_2 optimal dual-rate DT problem.

The plant $\widehat{G}(z,h)$ obtained in *step 2* can be placed in closed-loop with $\widehat{C}(z,h)$, which is the DT controller to be designed. The resulting closed-loop system can be expressed in the standard block diagrams shown in Figure 3. The dual-rate digital redesign problem can then be formulated as follows: Given a fast DT control system, design a dual-rate DT control system, as shown in Figure 4, such that its closed-loop step responses optimally match those of the fast DT control system by minimizing J given by (3).

$$J = \sum_{k=0}^{\infty} |z_1(k,h)|^2 + |z_2(k,h)|^2 \tag{3}$$

Remarks 1) From Figure 3, it should be noted that the blocks $H_{h,T}$, $\widetilde{H}_{h,T}$, S_h and S_h^g impact on the performance of the closed-loop system and that the selection of such blocks is an integral part of the design process. 2) The DT H_2 problem can be solved by using algebraic Riccati equations or LMI techniques, although the solution method constrains the construction of the generalized plant. For example, with the generalized plant $\widehat{G}(z,h)$ given as

$$\widehat{G}(z,h) = \left[\begin{array}{c|cc} A_G & B_1 & B_2 \\ \hline C_1 & D_{11} & D_{12} \\ C_2 & D_{21} & D_{22} \end{array}\right], \tag{4}$$

and forming algebraic Riccati equations to solve the H_2 problem, D_{12} and D_{21}^{T} must have full column rank. Furthermore, the pair (A_G, B_2) must be stabilizable and (C_2, A_G), detectable [10]. Hence, $\widehat{G}(z,h)$ must reflect these requirements; for instance, by appropriately selecting $H_{h,T}$, $\widetilde{H}_{h,T}$, S_h and S_h^g 3) The resulting controller $\widehat{C}(z,h)$ is strictly proper. 4) With the presence of $\widetilde{H}_{h,T}$ and S_h^g in the generalized plant, a certain amount of information on the fast DT signals is carried over to the DT H_2 problem. 5) As shown in Figure 2, signal $z_2(k,h)$ comprises the weight factor ρ.

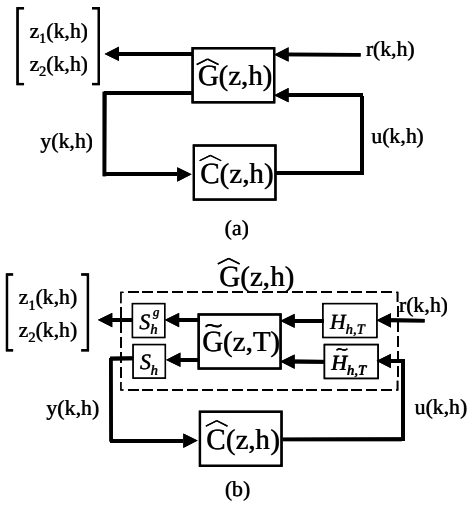

Figure 3: Equivalent block diagrams for controller synthesis

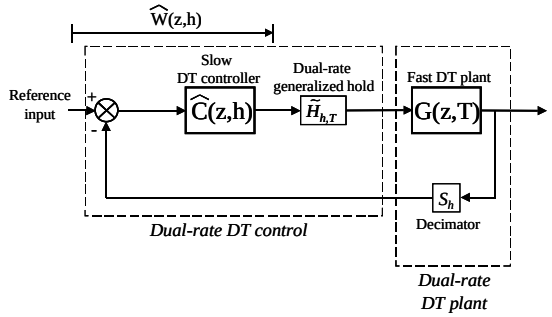

Figure 4: Dual-rate DT control system

STEP 4: DT controller order reduction.

If required, the order of $\widehat{C}(z,h)$ can be reduced as follows.

Step 4.1: Calculate the plant-input transfer function (PITF) $\widehat{W}(z,h)$, which relates the reference input to the input to $\widetilde{H}_{h,T}$, as shown in Figure 4.

Step 4.2: Continualize the DT PITF $\widehat{W}(z,h)$ to $\widehat{W}(s)$ using Tustin's method [1].

Step 4.3: Select the order of the desired PITF, taking into account the order of the fast DT plant.

Step 4.4: Apply balanced-truncation model reduction [13] to the CT PITF $\widehat{W}(s)$ to obtain $\widehat{W}_{reduced}(s)$ with the order set in *step 4.3*.

Step 4.5: Discretize $\widehat{W}_{reduced}(s)$ to $\widehat{W}_{reduced}(z,h)$ using the matched pole-zero method [1].

Step 4.6: Modify the numerator of the DT PITF $\widehat{W}_{reduced}(z,h)$ to account for the feedback effect while preserving the low-frequency or DC gain. The resulting DT PITF is termed $\widetilde{W}_{reduced}(z,h)$. To obtain $\widetilde{W}_{reduced}(z,h)$, one can proceed as follows. First, include the poles of the slow system $S_h G \widetilde{H}_{h,T}$ as zeros of $\widetilde{W}_{reduced}(z,h)$. Second, keep the zeros of $\widehat{W}_{reduced}(z,h)$ closest to the unit circle as zeros of $\widetilde{W}_{reduced}(z,h)$. The number of finite zeros of $\widetilde{W}_{reduced}(z,h)$ depends on the degree of the numerator polynomial of $\widehat{W}_{reduced}(z,h)$, which should be preserved in the transformation to $\widetilde{W}_{reduced}(z,h)$. Third, adjust the low-frequency or DC gain of $\widetilde{W}_{reduced}(z,h)$ to match that of $\widehat{W}_{reduced}(z,h)$.

Step 4.7: Compute the DT controllers from the knowledge of $\widetilde{W}_{reduced}(z,h)$. The controllers are obtained by using the so-called plant input mapping method [8]. The resulting closed-loop system is shown in Figure 5, where each controller $\widetilde{A}(z,h)$, $\widetilde{B}(z,h)$ and $\widetilde{C}(z,h)$ may be a gain or a dynamic system.

Remarks 1) Steps 4.1 to 4.7 form a closed-loop order-reduction technique that warrants closed-loop stability by the consideration of the PITF. 2) Steps 4.6 and 4.7 are based on the concept of plant input mapping, which is an approach to digital redesign originating from [8] and which is used here, for the first time, to reduce the complexity of a DT control system.

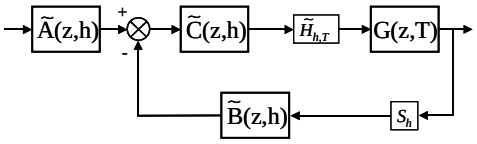

Figure 5: Dual-rate DT control system with order reduction

III. NUMERICAL EXAMPLES

A. BENCHMARK CONTROL SYSTEM

Consider the linear, time-invariant CT control system used in [9] with the structure of Figure 1(a) and $\overline{A}(s)=1$, $\overline{B}(s)=1$,

$$\begin{aligned}\overline{C}(s) &= \tfrac{s^2+10.42s+20}{s^2+32.44s+20}\\ \overline{G}(s) &= \tfrac{20}{s(1+s/10)(1+s/30)}.\end{aligned} \tag{5}$$

Digital redesign is performed using the optimal method of [9], the Tustin's method (on $\overline{C}(s)$), and the proposed approach. For $h=0.4$, the DT controllers obtained with the proposed method are

$$\begin{aligned}\widetilde{A}(z,h)=0.1229,\ \widetilde{B}(z,h) &= \tfrac{0.085z-0.0025}{z-0.33}\\ \widetilde{C}(z,h) &= \tfrac{z-0.33}{z+0.1594},\end{aligned} \tag{6}$$

local discretization of $\overline{C}(s)$ using Tustin's method results in

$$\widetilde{C}(z,h) = \tfrac{z^2-1.746z+0.7639}{z^2-1.2553z+0.2732} \tag{7}$$

and the optimal method of [9] yields

$$\widetilde{C}(z,h) = \tfrac{0.1625z^4-0.066z^3+0.00685z^2+0.000104z-0.0000044}{z^4-0.09196z^3-0.118z^2+0.01477z-0.00056}. \tag{8}$$

Figure 6 shows the step responses obtained with the CT control system and the single-rate SD control systems, where the DT controllers have a sampling period $h=0.4$.

The proposed approach results in a SD control system with response having the smallest overshoot, the fastest settling time, albeit having the longest rise time. The method of [9] results in a SD system having the closest step response to that of the CT control system. Tustin's method fails to preserve closed-loop stability. Figure 7 shows the responses to a unit-step disturbance applied at time $t = 1$. The SD system obtained with the proposed method shows a disturbance response free of undershoot, although it presents the longest settling time when compared with the response obtained with the method of [9]. From (5)-(8), the proposed approach results in the smallest controller order, an order selected by the designer, although it results in a three-controller SD system whereas the nominal CT control system comprises a single controller.

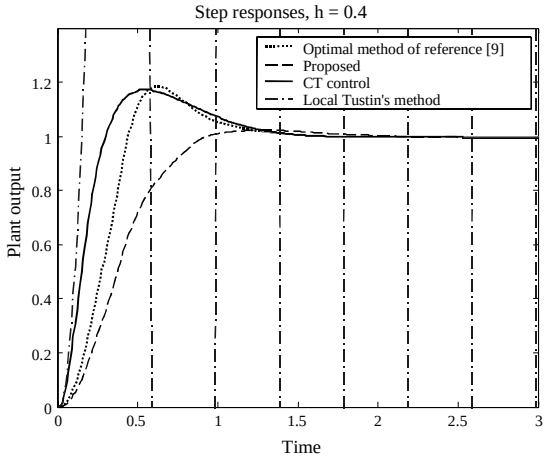

Figure 6: Step responses

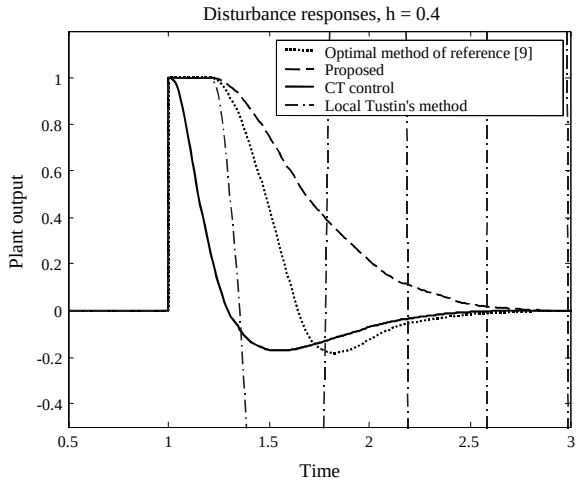

Figure 7: Disturbance responses

B. ACCELERATION AUTOPILOT

Consider a symmetrical, tail-controlled missile. Pitch plane dynamics can be linearized at an altitude of 500 m and a speed of Mach 4 to yield the following linear models

$$\begin{array}{l} \frac{q(s)}{\delta_p(s)} = \frac{-1354.99s-3865.92}{s^2+6.907s+726.43} \\ \frac{a_z(s)}{\delta_p(s)} = \frac{1\times10^6(-0.001s^2-0.0038s+5.23)}{s^2+6.907s+726.43} \end{array} \quad (9)$$

where the signals correspond to perturbation variables. In (9), a_z corresponds to lateral acceleration, q is pitch rate resolved in the body coordinates and δ_p represents fin deflection in pitch. The linear CT missile acceleration autopilot is shown in Figure 8, where

$$\overline{C}(s) = \frac{3.5\times10^{-6}s + 1.28\times10^{-3}}{s}, \ \overline{K} = -0.0283. \quad (10)$$

Figure 9 presents the SD missile autopilot structure as obtained by applying the proposed dual-rate digital redesign method to the system of Figure 8. In Figure 9, H and S are the ZOH and the ideal sampler, respectively, with period T. With $K = \overline{K}$ and $h = 0.2$ ($N = 20$), the DT controllers are given as

$$C(z,h) = \frac{1\times10^{-4}(1.32z+1.25)}{z-1} \quad (11)$$

using Tustin's method and as

$$C(z,h) = \frac{1\times10^{-4}(2.25z^3+0.21z^2+0.0058z+0.000019)}{z^4+0.74z^3-1.59z^2-0.15z-0.0036} \quad (12)$$

for the proposed digital redesign.

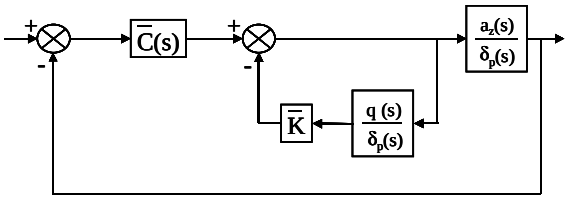

Figure 8: Two-loop CT missile autopilot

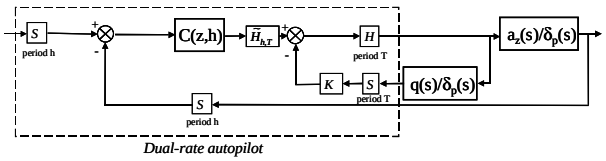

Figure 9: Dual-rate SD missile autopilot

Figures 10 and 11 show the responses of the SD and CT missile autopilots to a unit-step acceleration demand. The dual-rate SD systems execute at periods $T = 0.01$ and $h = 0.02$ ($N = 2$) in Figure 10, whereas $T = 0.01$ and $h = 0.2$ ($N = 20$) in Figure 11. From the figures, the SD control system obtained with the proposed digital redesign technique provides the best step-tracking performance. It should be pointed out that the step response obtained with the proposed method shows a one sample delay due to the fact that the controller is strictly proper.

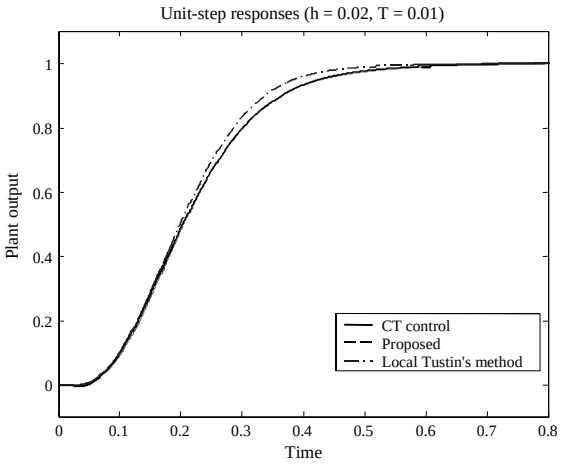

Figure 10: Unit-step responses of the control systems ($h = 0.02, T = 0.01$)

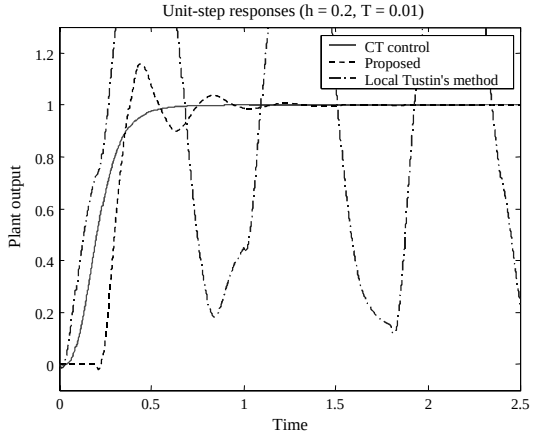

Figure 11: Unit-step responses of the control systems ($h = 0.2, T = 0.01$)

IV. CONCLUSIONS

The paper proposed optimal dual-rate digital redesign methods which rely on the solution of a dual-rate H_2 DT control problem. The proposed digital redesign techniques result in SD control systems providing satisfactory closed-loop performances, in terms of reference input tracking and disturbance rejection, over an extended range of sampling rates, as compared with other widely used methods of digital redesign. The latter was demonstrated with numerical examples. In practice, the proposed techniques are very useful since they allow the designer to constrain the complexity of the resulting digital controllers. Future research should investigate the robust dual-rate digital redesign problem and the mixed H_2/H_∞ redesign incorporating multiple design objectives.

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