2008 American Control Conference
Westin Seattle Hotel, Seattle, Washington, USA
June 11-13, 2008

Iterative Learning Control Design for Synchronization of Wafer and Reticle Stages

Sandipan Mishra, William Yeh, Masayoshi Tomizuka

Abstract— **This paper presents an iterative learning controller (ILC) design technique for synchronization in wafer scanning systems. In wafer scanners, synchronization of the wafer and reticle stages is critical for accurate pattern transfer. For synchronization, a master-slave configuration is used, with the wafer stage acting as the master, and the reticle stage as the slave. Since the scanning process is repetitive, ILC is used to improve tracking performance. However, the coupling between the reticle stage and wafer stage is unidirectional. Hence we propose an ILC scheme that takes into account this structural property of the overall system. A simple design procedure is presented which allows design of the ILC system for the wafer and reticle stages independently. This is done by first designing an ILC controller for the wafer (master) stage, and then using the synchronization error for ILC update for the reticle (slave) stage. Analytic conditions for stability and monotonic error convergence are then discussed. Finally, design and performance of the algorithm is illustrated by implementation on a single degree of freedom wafer stage, and a virtual (computer-simulated) reticle stage.**

I. Introduction

Photolithography is one of the central processes in semiconductor manufacturing. *Wafer Scanners* are optomechanical devices used for photolithography. As semiconductor technology becomes more sophisticated, better positioning accuracy is necessary for the wafer and reticle stages in wafer scanners. At the same time, in order to increase throughput, speed of positioning must also be improved. Hence, there is a growing need to introduce advanced control techniques for precision positioning of the wafer and reticle stages in photolithography machines. In a step-and-scan wafer scanner, the reticle and wafer stages are both driven to increase exposure length. However, the scanning process requires that the two stages be synchronized to within 10nm. Since synchronization of the two stages is important, having individual control loops around each of the wafer stages is inadequate. Therefore, a coordinated control system that synchronizes the stages while ensuring that the tracking error of each individual loop is small is used. Traditionally a master-slave scheme has been used for synchronization of the wafer and reticle stages[1]. In the master-slave synchronization scheme considered in [1], one of the stages acts independently (the master), and the other stage (slave) follows the motion of the master stage. The reticle stage typically has much higher bandwidth than the wafer stage, therefore it is chosen to be the slave stage, while the wafer stage acts as the master stage.

Considering the repetitive nature of scanning, iterative learning control (ILC) has been used extensively for improving trajectory tracking and repetitive disturbance rejection in wafer scanners [2], [3]. In more recent developments, ILC has also been used to generate improved trajectories [4] for wafer stage positioning.

ILC is loosely based on the paradigm of human *learning*. In a repetitive process, information from earlier iterations of the process can be used to improve performance in the current iteration. The key motivation behind the design of novel ILC schemes is the efficient use of information from previous iterations so as to maximize performance (minimize tracking error), increase robustness, and accelerate convergence rate. The early rigorous formulations of ILC were developed by Arimoto [5] and Uchiyama [6]. Arimoto [5] used a P-type ILC scheme for control of robotic manipulators. Since then, ILC has been implemented in several applications for control of repetitive processes because of its simplicity of design, analysis and implementation. In particular, it has been successfully implemented in industrial robots [7], [8], computer-numerical control tools [9], injection molding systems [10], rapid thermal processing [11], and micro-scale robotic deposition [12]. More recently, cross-coupled ILC design for contour tracking has been explored [13].

In wafer scanners, an added level of complexity enters the ILC design process as a result of the need for synchronization of the wafer and reticle stages. Multiple-input multiple-output (MIMO) ILC design [14] may be used in such applications. MIMO ILC design techniques are, however, difficult to tune. In this paper, we propose a simple ILC design technique for synchronization of the wafer and reticle stages, based on standard single-input single-output (SISO) ILC design techniques.

The rest of this paper is organized as follows. Section II introduces some notation. Section III presents the standard synchronization problem for the wafer and reticle stages. The standard ILC design problem is described in Section IV. Sections V and VI develop ILC design techniques and stability conditions for master-slave and general synchronization applications. Section VII describes the implementation of the ILC design scheme for synchronization, on a prototype setup. Finally, section VIII outlines the conclusions and open problems that need to be tackled.

Sandipan Mishra is a PhD Candidate in Mechanical Engineering, University of California, Berkeley, USA. sandipan@me.berkeley.edu

William Yeh is an undergraduate student in Mechanical Engineering, University of California, Berkeley, USA. wyeh@berkeley.edu

Masayoshi Tomizuka is with the Faculty in Mechanical Engineering, University of California, Berkeley, USA. tomizuka@me.berkeley.edu

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II. NOTATION

$P_i(z) =$ Plant model for wafer or reticle stage
$N =$ Period of the Repetitive Process
$F_k(j) =$ $(F)(kN+j)$
$r^0(j) =$ Reference trajectory for wafer stage
$y_{w,k} =$ Wafer stage position at step j, iteration k
$e_{w,k}(j) =$ Wafer stage following error at step j, iteration k
$e_{s,k}(j) =$ Synchronization error at step j, iteration k
$\|F\| =$ Standard 2-norm
$\rho(F) =$ Spectral Radius of the Matrix F
$W(z) =$ $\mathscr{Z}$-transform of the signal $w(j)$

III. SYNCHRONIZATION

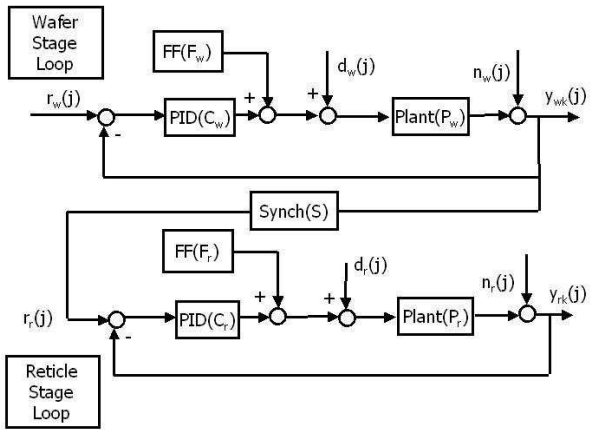

Fig. 1. Block diagram of a master-slave synchronization scheme

Figure 1 illustrates the overall synchronization control scheme for the wafer and reticle stages. The wafer stage position is regulated by a feedback and feedforward controller to follow the designed scanning trajectory ($r_w(j)$). For scanning, the reticle stage follows a scaled version of the wafer stage trajectory. The wafer and reticle stage feedback $(C_w(z), C_r(z))$ and feedforward $(F_w(z), F_r(z))$ controllers are designed keeping in mind the respective bandwidth, sensitivity and vibration suppression requirements. The sensor noise and disturbances for the wafer and reticle stages are denoted by $n_w(j), n_r(j)$ and $d_w(j), d_r(j)$.

The reticle stage is lighter and allows for higher bandwidth control loops as compared to the wafer stage. Considering the fact that the reticle stage loop has much higher bandwidth and smaller disturbances vis-a-vis the wafer stage loop, a master-slave synchronization scheme is used. In the master-slave synchronization scheme, the position measurement of the wafer stage is used to generate the reference trajectory for the reticle stage. The block $\mathbf{S}$ in Figure 1 represents the synchronization ratio. Therefore the overall system can be described by the following set of equations.

$$y_w(j) = T_w(z)r_w(j) + P_w(z)S_w(z)\left(d_w(j) + u_{fw}(j)\right)$$
$$y_r(j) = T_r(z)r_r(j) + P_r(z)S_r(z)\left(d_r(j) + u_{fr}(j)\right)$$
$$r_r(j) = \mathbf{S}y_w(j)$$

$$S_i(z) = \frac{1}{1+P_i(z)C_i(z)} \quad i \in \{w, r\} \tag{1}$$
$$T_i(z) = \frac{P_i(z)C_i(z)}{1+P_i(z)C_i(z)} \quad i \in \{w, r\} \tag{2}$$

$S_i(z), T_i(z)$ represent the sensitivity and complementary sensitivity functions respectively for the wafer and reticle stages. The overall control system must minimize the trajectory following error for the wafer stage $\left(e_w(j) = r_w^0(j) - y_w(j)\right)$, and the synchronization error between the wafer and the reticle stage $(e_s(j) = \mathbf{S}y_w(j) - y_r(j))$.

The wafer and reticle stages execute the scanning process repetitively with a period of N samples. The scanning system comes back to rest at the end of each iteration of the cycle, and starts from rest condition at the beginning of each iteration. We will add a subscript k to designate the iteration number as shown in Figure 2, i.e.,

$$y_{w,k}(j) = T_w(z)r_{w,k}(j) + P_w(z)S_w(z)\left(d_w(j) + u_{fw}(j)\right)$$
$$y_{r,k}(j) = T_r(z)\left(r_{r,k}(j) + \mathbf{S}y_{w,k}(j)\right) + P_r(z)S_r(z)\left(d_r(j) + u_{fr}(j)\right)$$
$$r_{r,k}(j) = \mathbf{S}y_{w,k}(j)$$

Note that the reference to the reticle stage has two components, the scaled wafer stage position $\mathbf{S}y_{w,k}(j)$ and the learning signal $r_{r,k}(j)$.

IV. ITERATIVE LEARNING CONTROL FOR SISO SYSTEMS

Let us consider a *stable* discrete time linear time invariant single-input single-output (SISO) system, denoted by $G(z^{-1})$. This system executes a repetitive process with period of N samples. We want the output of the system to track a trajectory $r(j)$, where j ranges from 0 to $N-1$. This is repeated several times, with the system coming back to rest condition at the end of each iteration of the cycle, and starting at rest condition at the beginning of each iteration. The output of the plant for each iteration is denoted by $y_k(j)$, where j ranges from 0 to $N-1$, and k denotes the iteration number. Therefore, we have the following relationship

$$Y_k(z) = G(z^{-1})(R_k(z) + D(z)) \tag{3}$$
$$E_k(z) = R(z) - Y_k(z) \tag{4}$$

where $R_k(z)$ is the Z-transform of input to the plant $r_k(j)$, and $E_k(z)$ is the Z-transform of the error from the desired trajectory.

The standard SISO ILC design problem can then be formulated as:

$$R_{k+1}(z) = R_k(z) + L(z)E_k(z) \tag{5}$$

$L(z)$, the learning filter, must be designed so that the ILC loop is stable.

Definition: [15] (asymptotic stability): A system using ILC is asymptotically stable if

$$lim_{k\to\infty} \left\| R_{ss}(e^{j\omega}) - R_k(e^{j\omega}) \right\| \to 0 \tag{6}$$

This is guaranteed if $\|1-L(z)G(z)\|_\infty < 1$. The standard SISO ILC design problem has been well-researched in literature [15].

Remark 1: If $\|1-L(z)G(z)\|_\infty < 1$, it can further be said that the error converges *monotonically*. This is a desirable property for avoiding bad learning transient.

V. Iterative Learning Control for Master-Slave Synchronization

In this section, an ILC design strategy is developed for the wafer and reticle stages, with a master-slave synchronization structure embedded in the inner loop. The overall system now has two inputs ($r_{w,k}(j)$, $r_{r,k}(j)$) and two measured outputs that can be used for learning, ($y_{w,k}(j), y_{r,k}(j)$). The two performance objectives are to minimize waferstage tracking error ($e_{w,k}(j)$) and synchronization error ($e_{s,k}$) between the wafer and reticle stages.

MIMO ILC techniques can be used for designing learning schemes. However, intuitive design and tuning of MIMO ILC is difficult, therefore we propose a design technique that decomposes this MIMO ILC problem into *two* SISO ILC design problems.

The ILC scheme is implemented as an add-on feature around the standard feedforward and feedback loops. Wafer stage tracking error, and synchronization error are the signals used for improving performance in the next cycle. This performance enhancement is obtained by changing the *reference* inputs of each loop, i.e., $r_{w,k}(j)$ and $r_{r,k}(j)$. Figure 2 shows the overall control system excluding the ILC loops. The learning signals are $e_{s,k}(j)$ and $e_{w,k}(j)$.

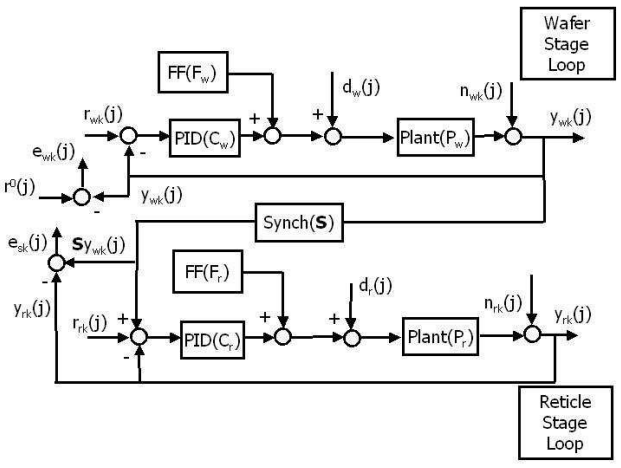

Fig. 2. Block diagram of a master-slave synchronization scheme with ILC loop

The ILC update law for both $R_{w,k}(z)$ and $R_{r,k}(z)$ is

$$R_{w,k+1}(z) = R_{w,k}(z) + L_{11}(z)E_{w,k}(z) + L_{12}(z)E_{s,k}(z) \quad (7)$$

$$R_{r,k+1}(z) = R_{r,k}(z) + L_{21}(z)E_{w,k}(z) + L_{22}(z)E_{s,k}(z) \quad (8)$$

$$E_{w,k}(z) = R^0(z) - Y_{w,k}(z)$$

$$E_{s,k}(z) = \mathbf{S}Y_{w,k}(z) - Y_{r,k}(z)$$

Eqs. 7 and 8 can be combined with the plant equations to obtain the error evolution equations shown below.

$$E_{w,k+1}(z) = (1-T_w(z)L_{11}(z))E_{w,k}(z) - T_w(z)L_{12}(z)E_{s,k}(z)$$

$$E_{s,k+1}(z) = (\mathbf{S}(1-T_r(z))T_w(z)L_{11}(z) - T_r(z)L_{21}(z))E_{w,k}(z) + (1+\mathbf{S}(1-T_r(z))T_w(z)L_{12}(z) - T_r(z)L_{22}(z))E_{s,k}(z)$$

In matrix form, we can write this as

$$\begin{bmatrix} E_{w,k+1}(z) \\ E_{s,k+1}(z) \end{bmatrix} = \begin{bmatrix} M_{11}(z) & M_{12}(z) \\ M_{21}(z) & M_{22}(z) \end{bmatrix} \begin{bmatrix} E_{w,k}(z) \\ E_{s,k}(z) \end{bmatrix}$$

where $M(z) =$

$$\begin{aligned} M_{11}(z) &= 1 - T_w(z)L_{11}(z) \\ M_{12}(z) &= -T_w(z)L_{12}(z) \\ M_{21}(z) &= \mathbf{S}(1-T_r(z))T_w(z)L_{11}(z) - T_r(z)L_{21}(z) \\ M_{22}(z) &= 1 + \mathbf{S}(1-T_r(z))T_w(z)L_{12}(z) - T_r(z)L_{22}(z) \end{aligned}$$

Theorem 1: [15] The synchronized ILC scheme is stable if $\rho(M(z)) < 1, \forall z = e^{j\omega}$.

Remark 2: Further, we can guarantee monotonic convergence of the error if $\bar{\sigma}(M(z)) < 1, \forall z = e^{j\omega}$.

ILC Design Scheme for Synchronization

We propose a simple design method based on Theorem 1 that guarantees *monotonic* convergence of the synchronization and waferstage tracking error. The learning filters $L_{ij}(z)$ are chosen as

$$L_{11}(z) = T_r(z)L_0(z), \quad L_{12}(z) = 0$$

$$L_{21}(z) = \mathbf{S}(1-T_r(z))T_w(z)L_0(z)$$

For this choice of learning filters, the matrix $M(z)$ reduces to

$$\begin{bmatrix} 1-T_w(z)T_r(z)L_0(z) & 0 \\ 0 & 1-T_r(z)L_{22}(z) \end{bmatrix}$$

$L_0(z)$ is chosen such that

$$\|1-T_w(z)T_r(z)L_0(z)\|_\infty < \gamma_1 < 1 \quad (9)$$

$L_{22}(z)$ is chosen such that

$$\|1-T_r(z)L_{22}(z)\|_\infty < \gamma_2 < 1 \quad (10)$$

The choice of the learning gains is explained below.

$L_{12}(z) = 0$ decouples the the MIMO system into two SISO problems. However, it does not guarantee monotonic convergence of each loop. $L_{21}(z)$ chosen as above is a *predicitive* term for the reticle stage loop in anticipation of the change of trajectory of the wafer stage. Therefore, it helps in completely decoupling the two systems and allows monotonic convergence of both the waferstage error and the synchronization error. $L_{11}(z)$ and $L_{22}(z)$ are chosen such that we avoid inversion of the individual loop dynamics $T_w(z)$ and $T_r(z)$.

Remark 3: The synchronization ILC learning problem therefore is reduced to two *decoupled* SISO ILC design problems.

We can use standard SISO ILC design techniques to satisfy equations 9 and 10. Further, we can adjust the *rate of learning* for each loop (γ_1 and γ_2) individually.

Remark 4: For stability of the ILC scheme, it is sufficient to design $L_{12}(z) = 0$, while $L_{21}(z)$ may be chosen arbitrarily. This choice of the learning filters, however, does not guarantee monotonic convergence.

VI. Iterative Learning Control for General Synchronization Structures

In this section, an extension of the ILC design strategy proposed in Section V that guarantees monotonic error convergence for the general synchronization problem is developed. We will not assume the unidirectional coupling structure as in master-slave synchronization. The general form for the overall ILC system for this problem can be written as:

$$\begin{bmatrix} R_{1,k+1}(z) \\ R_{2,k+1}(z) \end{bmatrix} = \begin{bmatrix} R_{1,k}(z) \\ R_{2,k}(z) \end{bmatrix} + \begin{bmatrix} L_{11}(z) & L_{12}(z) \\ L_{21}(z) & L_{22}(z) \end{bmatrix} \begin{bmatrix} E_{1,k}(z) \\ E_{2,k}(z) \end{bmatrix}$$

$$\begin{bmatrix} E_{1,k}(z) \\ E_{2,k}(z) \end{bmatrix} = \begin{bmatrix} R_0(z) \\ 0 \end{bmatrix} - \begin{bmatrix} T_{11}(z) & T_{12}(z) \\ T_{21}(z) & T_{22}(z) \end{bmatrix} \begin{bmatrix} R_{1,k}(z) \\ R_{2,k}(z) \end{bmatrix}$$

$$\Rightarrow \begin{bmatrix} E_{1,k+1}(z) \\ E_{2,k+1}(z) \end{bmatrix} = M(z) \begin{bmatrix} E_{1,k}(z) \\ E_{2,k}(z) \end{bmatrix}$$

$$M(z) = I - \begin{bmatrix} T_{11}(z) & T_{12}(z) \\ T_{21}(z) & T_{22}(z) \end{bmatrix} \begin{bmatrix} L_{11}(z) & L_{12}(z) \\ L_{21}(z) & L_{22}(z) \end{bmatrix}$$

We propose a simple design method for the general coupled ILC problem above, based on the theorem in Section V. The choice of the learning filters $L_{ij}(z)$ is such that the off diagonal terms in $M(z)$ are set to zero.

$$L_{11}(z) = T_{22}(z)L_{01}(z), \quad L_{12}(z) = -T_{12}(z)L_{02}(z)$$
$$L_{21}(z) = -T_{21}(z)L_{01}(z), \quad L_{22}(z) = T_{11}(z)L_{02}(z)$$

For this choice of learning filters, the matrix $M(z)$ reduces to

$$M_{11}(z) = 1 - (T_{11}(z)T_{22}(z) - T_{12}(z)T_{21}(z))L_{01}(z) \quad (11)$$
$$M_{12}(z) = M(z)_{21} = 0 \quad (12)$$
$$M_{22(z)} = 1 - (T_{11}(z)T_{22}(z) - T_{12}(z)T_{21}(z))L_{02}(z) \quad (13)$$

In order to make the ILC loop *monotonically* stable, $L_{01}(z)$ is chosen such that

$$\|1 - (T_{11}(z)T_{22}(z) - T_{12}(z)T_{21}(z))L_{01}(z)\|_\infty < 1 \quad (14)$$

and, $L_{02}(z)$ is chosen such that

$$\|1 - (T_{11}(z)T_{22}(z) - T_{12}(z)T_{21}(z))L_{02}(z)\|_\infty < 1 \quad (15)$$

As in the previous case, we can now design $L_{01}(z)$ and $L_{02}(z)$ separately using standard SISO ILC design techniques. Further, if $T_{12}(z) = 0$, then this problem reduces to the master-slave synchronization ILC problem discussed earlier in Section V.

VII. Experimental Setup and Results

A. Experimental Setup

The experimental prototype wafer stage, shown in Figure 3, includes a stage and countermass system, both driven by linear motors. The stage is mounted on air-bearings and the countermass is guided by roller bearings. Stage position is measured by a laser interferometer, and the countermass position is measured using a linear encoder. Though not shown, power cables and pneumatic tubing are among the potential sources of disturbances to the stage. The prototype wafer stage can be modeled as a simple mass-damper system as below.

$$P_w(s) = \frac{11.79}{5.3s^2 + 7.2s} \quad (16)$$

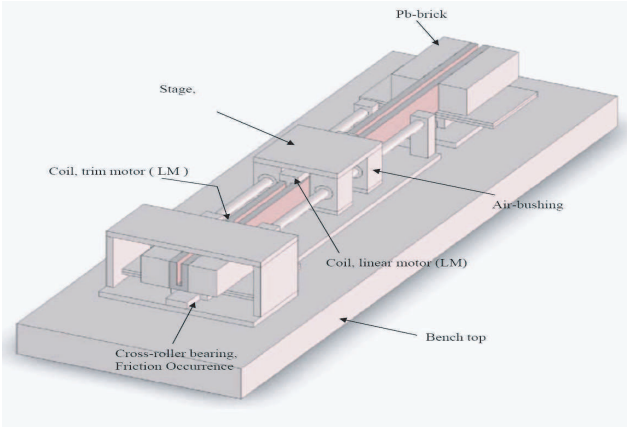

Fig. 3. Schematic of stage/countermass system.

The reticle stage is simulated as a virtual machine, running in parallel operation with the prototype wafer stage. The reticle stage is also modeled as a simple mass-damper system.

$$P_r(s) = \frac{10.1}{1.0s^2 + 0.12s} \quad (17)$$

The reference trajectory for the wafer stage is designed as shown in Figure 4. This trajectory replicates the movement of one of the axes of a wafer stage. The goal is to achieve constant velocity as soon as possible to within a certain accuracy so that scanning can be performed. This imitates one scan, which is then repeated to produce the same pattern on multiple ICs. The virtual reticle stage follows a scaled version of this reference trajectory, with scaling factor (**S**) 4. This is a typical trajectory for the reticle stage for scanning.

Feedback PID controllers $C_w(z^{-1})$ and $C_r(z^{-1})$ were designed for the wafer stage keeping in mind the bandwidth and sensitivity constraints for both stages respectively. The sampling time of the controller was set to $400\mu s$. Inertial feedforward was used to improve the transient response of the overall system.

B. Results

In order to improve tracking and synchronization performance of the wafer and reticle stages, an ILC loop was

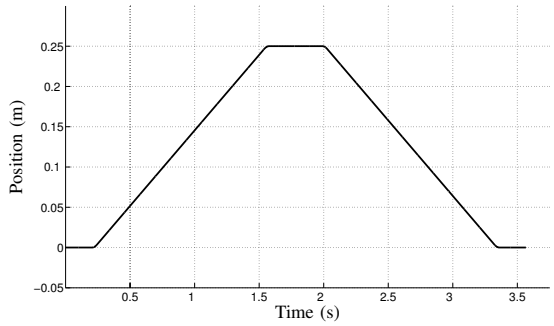

Fig. 4. Reference trajectory for wafer stage

implemented around both stages, as shown in Figure 2. The ILC learning filters were designed based on the constraints developed in section V, as below

$$L_0(z) = 0.7z^6, \quad L_{22}(z) = 0.8z^3$$
$$L_{11}(z) = T_r(z)L_0(z), \quad L_{12}(z) = 0$$
$$L_{21}(z) = \mathbf{S}(1 - T_r(z))\,T_w(z)L_0(z)$$

where $T_r(z)$ and $T_w(z)$ were obtained from the plant and controller models of the reticle and wafer stages respectively. $L_0(z)$ and $L_{22}(z)$ satisfy equations (9) and (10).

The wafer stage following error for iterations 0, 3, and 6 is shown in Figure 5. The major source of following error during scanning is the force ripple. On the other hand, during the acceleration phase, the main cause of following error is phase-mismatch. Within 6 iterations, peak following error during the scanning phase is under 100nm. A detail of the following error during the scanning phase is shown in Figure 6.

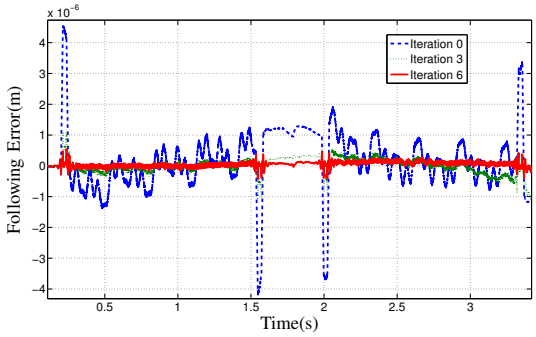

Fig. 5. Following error for wafer stage for iterations 0,3, and 6.

The synchronization error between the wafer and reticle stages for iterations 0, 3, and 6 is shown in Figure7. The initial cycle synchronization error is of the order of $300\mu m$. This is expected because of the inherent delay in the controller for the reticle stage. The ILC synchronization input to the reticle stage loop improves performance by compensating for this expected delay in the reticle stage controller. Monotone convergence (in the 2-norm sense) in

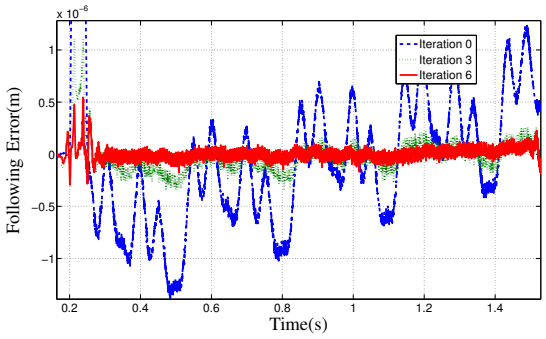

Fig. 6. Detailed view of following error for wafer stage during constant-velocity scanning, for iterations 0,3, and 6.

TABLE I
ERROR CONVERGENCE OVER ITERATIONS.

Iteration	Wafer stage tracking error $(2-norm)$	Synchronization error $(2-norm)$
0	93×10^{-5}	20×10^{-3}
1	72×10^{-5}	93×10^{-4}
2	49×10^{-5}	40×10^{-4}
3	35×10^{-5}	24×10^{-4}
4	26×10^{-5}	13×10^{-4}
5	18×10^{-5}	73×10^{-5}
6	16×10^{-5}	66×10^{-5}

observed in both the wafer stage following error, as well as the synchronization error. This is shown in Table I.

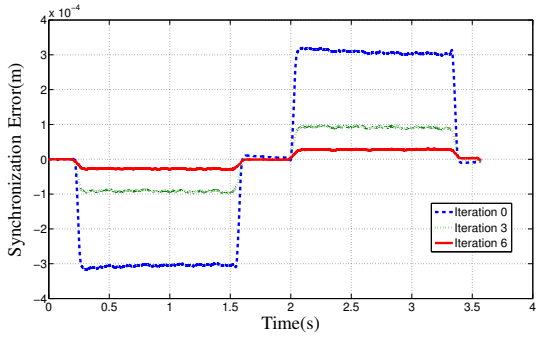

Fig. 7. Synchronization error between wafer and reticle stages for iterations 0,3, and 6.

VIII. CONCLUSIONS

Wafer scanning requires ultra-high precision positioning capabilities. In addition to smart design techniques, advanced control schemes are important for achieving the stringent performance standards. For uniform exposure, the wafer stage must scan at a constant velocity. In addition, for effective pattern transfer, the wafer and reticle stages must execute a coordinated and synchronized motion. For this purpose, a master-slave synchronization scheme is used. Since the scanning process is repetitive, ILC is used to improve performance. In this paper, we proposed an ILC

design procedure for synchronization. The coupling between the reticle stage and wafer stage is unidirectional, because of the master-slave synchronization scheme. We proposed an ILC scheme that takes into account this structural property of the overall system. A simple design procedure was presented which allowed design of the ILC system for the wafer and reticle stages independently. Analytic conditions for stability and monotonic error convergence were determined. This idea was then extended to ILC design for the general synchronization problem. Finally, design and performance of the algorithm was illustrated by implementation on a single degree of freedom wafer stage, and a virtual (computer-simulated) reticle stage. The major advantage of the proposed design method is that MIMO ILC design techniques are not needed, even though the overall system is no longer SISO.

There remain several open questions regarding robustness of the proposed scheme to uncertainty in the plant models for the wafer and reticle stages. Optimal choice of the learning filters based on some cost function is also another possible direction for future research. Investigation into incorporating model uncertainty for each loop into the learning algorithm is also an area of future research. An interesting extension of this work would be in the direction of ILC design for multi-agent systems.

ACKNOWLEDGMENTS

The authors gratefully acknowledge the contribution of Nikon Research Center of America. This project is funded by UC Discovery Grant # ele-10197.

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