

A New Cell Balancing Architecture for Li-ion Battery Packs Based on Cell Redundancy

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Abstract: Li-ion batteries are promoting the development of more and more performing electric vehicles (EVs) and hybrid EVs (HEVs). Thanks to their high energy density and increased current capabilities - which permit to use a relative light and space saving battery pack- these batteries are replacing almost all older battery chemistries in vehicle applications. Despite the advantages these cells provide, before use them in a new design, several drawbacks about safety aspects have to be considered. In fact, Li-ion battery packs require, more than other chemistry base packs, special control systems to maintain the operative conditions in a safe area and to guarantee the best performances in terms of efficiency and pack life time. One of the most challenging problems that have to be tackled by the mentioned control system is the voltage unbalance. This problem arises when more cells are connected in series with the purpose to increase the battery pack voltage. In this paper a new cell balancing architecture based on cell redundancy is proposed. This solution is especially suited to be implemented in vehicle battery management system (BMS) where cost and space reduction are the main requirements.

1. INTRODUCTION

The priority of electric vehicles as a primary factor of sustainable mobility is widely recognized worldwide also in the low-power two-wheels segment, i.e. scooters and bikes.

Lithium-ion (Li-ion) batteries, thanks to their high energy density, are commonly used for portable utilities and industry applications. Since voltage of a single cell is generally too low, for many high power applications such as electric vehicles (EVs), hybrid EVs (HEVs) plug-in HEVs (PHEVs), electric scooters, bikes, wheelchairs, and so on, string cells are often used. In this configuration, since the voltage of each cell can slightly vary with respect to the others, the problem of cell imbalance can arise. In fact, during the charge phase, due to different internal resistance, chemical variations and temperature gradient along the pack, can happen that some cells reach the full charge condition before others, and, most important, before the entire pack charge is completed. This situation, if unmanaged, could determine overcharge of some cells and undercharge of some others. In the same way, during the discharge phase, some cells can experience over-discharge whereas others could still store available energy.

Moreover, the repetition of charge/discharge cycles increases the voltage imbalance, which is particularly detrimental in EV applications because of charge/discharge dynamics. In fact, unlike standard applications where almost complete charge/discharge phases follow one another, in EV use (except for PEHV) charge/discharge phases are partial and interleaved. This is due to the fact that discharge occurs during acceleration and drive whereas charge during regenerative braking (A. Emadi 2008). This voltage imbalance, although can be detrimental regardless the battery chemistry, is particularly harmful for Li-ion battery. In fact, it

is well known that Li-ion batteries, like other chemistries, have both maximum and minimum voltage limit, which depend on specific cell. In this case however, exceeding these limits could entail severe safety problems since these batteries have no natural gassing mechanism to release an excess of energy with consequent explosion risk (H.V. Venkatesetty 2002). For this reason, a charge/discharge equalization procedure able to considerably improve the maintenance in time of cells efficiency is fundamental in case of vehicle Li-ion battery packs.

Many architectures have been proposed in order to prevent cell imbalance during charge/discharge of series-connected battery packs (Affanni October, 2005), (N. H. Kutkut 1999), (Ferdowsi 2005), (C. S.Moo 2003) and (J. Chatzakis 2003). Each of these solutions aims to a specific goal such as cost reduction, space saving (P. Casasso 2003), robustness, and so on. We present a new balancing approach that is suited for battery packs made up of a maximum 10 Li-ion cells for low-medium power applications (in the range from 100W to 500W). This solution can be oriented to light electric vehicles (i.e. electric bicycles), which usually need low-medium voltage (24V-36V) and current (10A) associated to a simple, inexpensive and space-saving layout. In agreement with classification proposed in (Hong-Sun Park 2009), we focused on non-dissipative bidirectional equalizers. First of all, this means that the proposed solution doesn't use extra-power to prevent imbalance, thereby increasing the overall efficiency. In addition, it continues to work during both charge and discharge operation phases, improving balancing effectiveness. The proposed strategy is based on the availability of an additional cell that can be continuously disconnected from the load. In this way, the bypassed cell is

isolated and can be optimally balanced while the remainder of the pack continues to provide energy to the load. It has to be notice that while pack works -charge or discharge- at least one cell is always disconnected from the string.

There are three main features of the proposed architecture. First, balancing is active both in charge and discharge phase. Second, the system layout is considerably space saving, which is a primary task for two-wheel vehicle applications often subjected to hard space constraints. Third, the solution offers an intrinsic hardness to a cell fault. In fact, if the pack should contain a cell with a severe fault, the control system can identify and bypass it permanently.

2. ARCHITECTURE

The balancing system has been designed bearing in mind a general-purpose application, both in terms of cell type and operating conditions. So, standard Lithium-Ion cells with the following features have used as reference:

- 4.2 V of full charge voltage
- 4400 mAh of capacity
- 10 A of maximum continuous current load
- 3 A of maximum charge current

All the system has been designed to manage a 7 cells battery pack. Consequently, it is able to manage a pack with a 25 V of open circuit voltage 10A of continuous load and nominal power of about 250W. Figure 1 shows the typical discharge profile of the used cell.

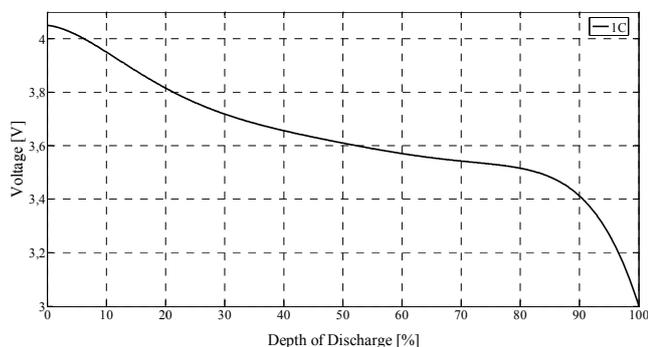


Figure 1: Typical discharge profile of a Lithium-Cobalt cell at 1C.

The block diagram of the experimental setup is shown in Figure 2. It is constituted by three main stages: the switch network -first responsible of the performance of the entire system-, the data acquisition block, and the control unit. In the following the switch network will be deeply analyzed whereas a detailed explanation of the other two blocks is beyond the scope of this paper.

A. Switch network

The switch network plays a crucial role since it is critical both from a safety and efficiency points of view. Even if at a first glance the structure and the operation modality of the circuit are simple (Figure 3), the implementation revealed several tricky issues both in layout and management algorithm.

In details:

- Since switches are connected in series on the load current path, their resistance directly impacts on performances (in terms of efficiency) of the system.
- Switches have to be able to interrupt current flow in both directions. In fact, the system must perform cell balancing both in charge phase, i.e. current flowing from external terminal to cells, and in discharge phase, i.e. current flowing from cells to external load.

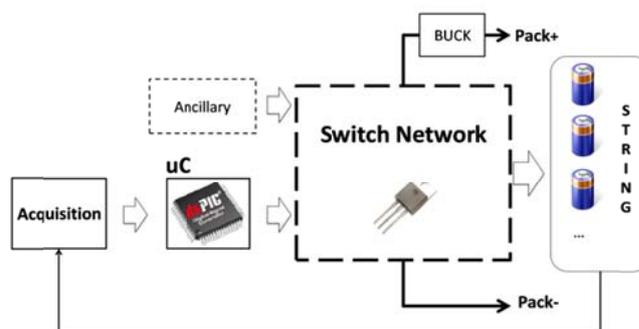


Figure 2: Block diagram of the proposed BMS architecture. Cores of the system are the data acquisition block (“Acquisition”), the control unit (the microcontroller “uC”), and the “Switch Network”.

- Topic of the implementation is to minimize the number of components, which also prevents the necessity to use specific drivers of switches.
- The system has to be safe in every operative condition, e.g. even if a single cell be physically taken out from pack or microcontroller stops for a while.

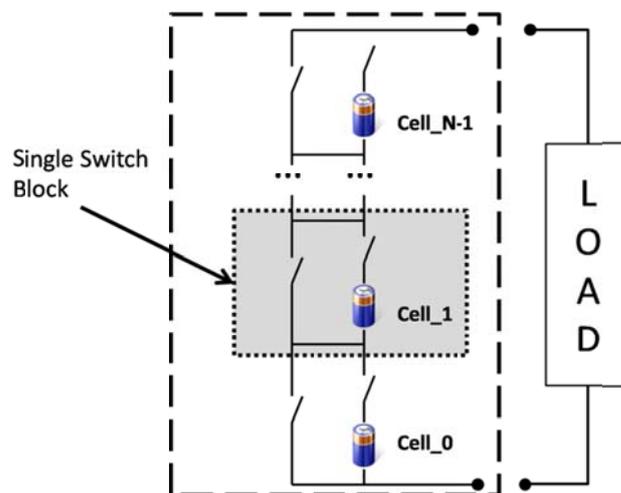


Figure 3: Basic representation of the switch network.

All these constraints make design of the stage critical both from layout and component choice points of view.

A simplified final schematic of the realized single switch between two adjacent cells is shown in Figure 4. Each cell has two switches, one series connected to the cell and the other one bypassing the cascade cell-switch. The single switch is constituted by two MOSFETs, in particular by N-channel MOSFETs (NMOS) for the series switch and by P-channel MOSFETs (PMOS) for the bypass switch. In this way, during

normal operation 6 cells are connected by NMOS switches and one cell is bypassed through a PMOS switch. This represents a significant advantage due to the lower on-resistance of NMOS compared with PMOS, which increases efficiency of the whole system.

This configuration results to be stable and safe also when command signals on gates of MOSFETs are floating due to control unit disconnection or initialization. This is achieved by using bipolar transistors in open-collector configuration in addition with a pull-up resistor to control the switches status. It should be noted that no specific driver circuits are used.

For border cells, i.e. bottom cell 0 and top cell $N-1$, switches architecture is quite different because gate command signal of MOSFETs cannot overcome rail voltage levels. So, bottom cell has both switches made by NMOS transistors. This solution makes the cell simpler to control and improves system efficiency. On the contrary, top switches use only P-channel transistors. In this case, the cell results harder to control. In fact, in case of control unit disconnection, terminals remain floating and both switches get opened. This required the addition of a Schottky diode at the top of pack able to provide automatic connection of cell $N-2$ to the output terminal in case of control unit disconnection.

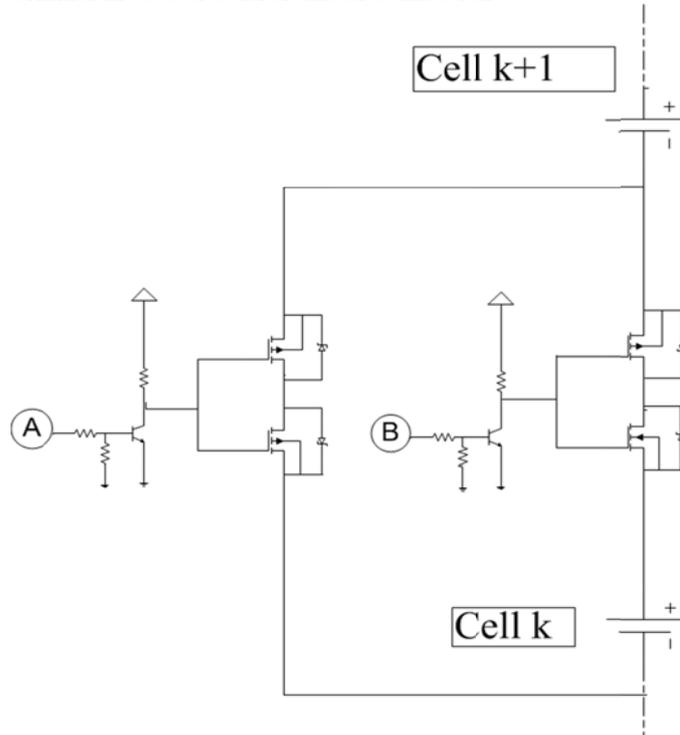


Figure 4: Simplified final schematic of a single switch block. A and B are the gates for control of the switch status by the control unit.

3. BALANCING ALGORITHM

The algorithm that manages cells connection or bypass represents another crucial part of the system. It directly impacts performance in terms of balance effectiveness and convergence speed. The algorithm has been developed bearing in mind to achieve requested performance with the simplest algorithm architecture. The flow chart of the developed algorithm is shown in Error! L'origine riferimento non è stata trovata.

First algorithm step is data acquisition where all needed signals are sampled (cell voltage, pack voltage, current). Core of the algorithm is the management of the cell to be disconnected, based on state of charge calculation of each battery. Several techniques for SoC estimation can be found in literature (V. Pop 2006), (V. Pop 2005) and (A. J. Salkind 1999). Unfortunately, most of them (e.g. OCV measurement, impedance spectroscopy, neural networks, fuzzy logic) are not suited to be used in this application, because some require battery disconnection or long resting times and some others need high amount of memory and computation resources. In this case the "Mixed Estimation Algorithm" (F. Codeca' Sept. 2008) has been adopted. This is the synthesis of Coulomb-Counting and Model-Based techniques and permits to minimize computation efforts maintaining accurate estimation results (F. Codeca' 2009) and (F. Codeca' 2009).

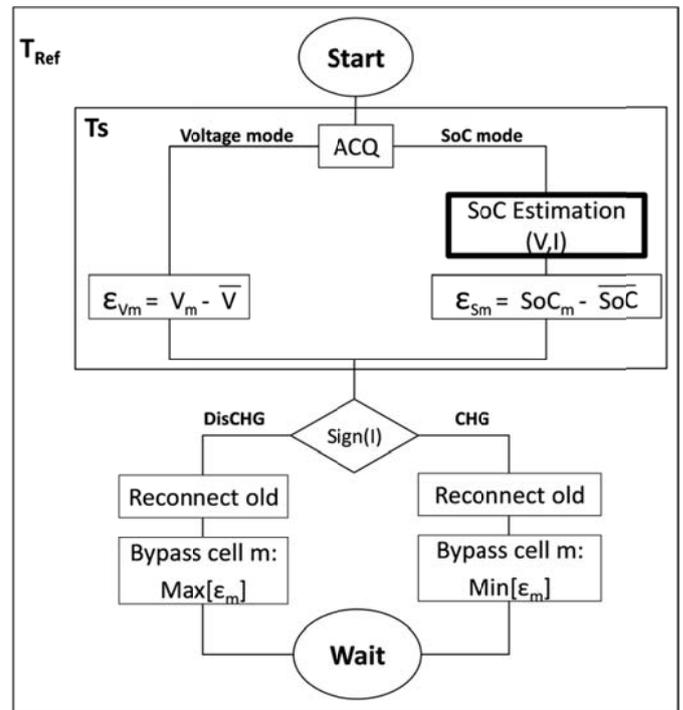


Figure 5: Developed algorithm flowchart

Here is explained the working principle of the decision strategy. As first step, the algorithm calculates the mean SoC over all the cells. Then, for each m -th cell it calculates the deviation ϵ_m of its SoC value with respect to the mean one. This deviation looks like:

$$\epsilon_{sm} = SoC_m - \overline{SoC} \quad (1)$$

Checking the current sign, algorithm establishes the working phase: if in discharge operation, cell with the lowest deviation is selected for disconnection, otherwise the one with the highest deviation value. The selected cell is bypassed and the previously bypassed one is re-connected into the string.

The algorithm runs cyclically. In particular, the first step and SoC estimation are performed with time interval T_s while pack configuration is updated with time interval T_{ref} (refresh time). For proper work, $T_{ref} \geq T_s$. Lowering T_s value increases the control bandwidth to prevent cell damage caused by over-voltages and under-voltages. On the contrary, T_{ref} is a critical parameter that hardly affects performance of the

system and whose optimal value will be discussed in next section.

4. PROTOTYPING

A picture of the realized prototype is shown in Figure 6.

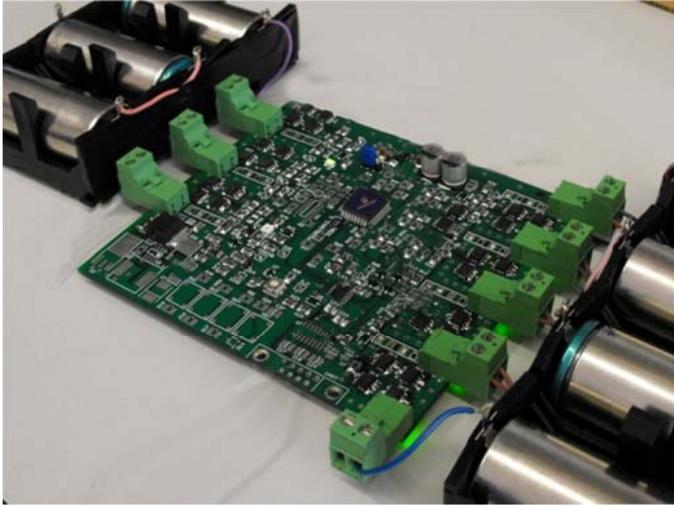


Figure 6: Picture of the circuit implementing the proposed BMS architecture.

A. Refresh time calculation

Data acquisition and SoC estimation are performed with time interval T_s while pack configuration is refreshed with time interval T_{ref} . Let us focus the influence of T_{ref} on system performance.

As T_s value doesn't impact on performance of the system as long as it remains small enough to allow an adequate acquisition rate, its value has been set constant to 2 seconds. On the contrary, T_{ref} is a critical parameter that hardly affects performance of the system: too large T_{ref} values correspond to a loss of balance accuracy, while too small T_{ref} values increase the stress of system and cells (e.g. due to current spikes associated to the reconfiguration process).

An analytical estimation of the best value of T_{ref} has been investigated. We consider a string of N perfectly balanced cells discharged at 1C. In order to compare performance obtained with different T_{ref} values, a figure of merit Q has been defined:

$$Q := \frac{1}{N} \sum_{m=0}^{N-1} \frac{1}{N} \int_0^{(N-1)T_{ref}} |\text{SoC}_m(t) - \overline{\text{SoC}}| dt \quad (2)$$

The parameter Q is the integrated absolute error in SoC, averaged across all the cells. This means that the balancing effect is much better as the Q factor decreases. Figure 7 graphically represents the terms of evaluation of eq. 2 for Q calculation in case of $N=7$ cells. Starting from the condition of all cells perfectly balanced with $\text{SoC}=\text{SoC}_i$ and considering the discharge phase of the pack, we consecutively disconnect one cell at a time for 7 consecutive reconfigurations. Figure 7 shows the superposition of SoC evolutions in time of a single cell – $\text{SoC}_2(t)$ –, and the SoC mean value of the entire pack $\overline{\text{SoC}}$. The horizontal step represents the transient of disconnection of the considered cell.

Numbering cells from 0 to $N-1$, SoC of each m -th cell depends on time as:

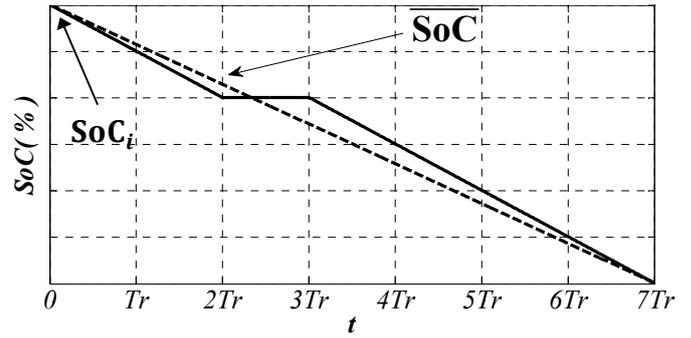


Figure 7: Trend of the SoCs during a period of seven consecutive reconfigurations. T_r is the refresh time and vertical axis represents SoC in arbitrary units.

$$\text{SoC}_m(t) = \begin{cases} \text{SoC}_i - t & t \in T1 \\ \text{SoC}_i - mT_{ref} & t \in T2 \\ \text{SoC}_i - mT_{ref} - (t - (m+1)T_{ref}) & t \in T3 \end{cases} \quad (3)$$

where

$$\begin{cases} T1 = 0 \leq t \leq mT_{ref} \\ T2 = mT_{ref} \leq t \leq (m+1)T_{ref} \\ T3 = (m+1)T_{ref} \leq t \leq NT_{ref} \end{cases} \quad (4)$$

The SoC mean value trend is a straight line described by the equation

$$\overline{\text{SoC}} = \text{SoC}_i - \left[\frac{N-1}{N} \right] t \quad (5)$$

Deviation $\Delta\text{SoC}_m(t)$ of the SoC of the m -th cell with respect to $\overline{\text{SoC}}$ results

$\Delta\text{SoC}_m(t)$

$$= \begin{cases} -\frac{1}{N}t & t \in T1 \\ -\frac{1}{N}mT_{ref} + \frac{N-1}{N}(t - mT_{ref}) & t \in T2 \\ \frac{N-1-m}{N}T_{ref} - \frac{1}{N}(t - (m+1)T_{ref}) & t \in T3 \end{cases} \quad (6)$$

and the mean value of $\Delta\text{SoC}_m(t)$ is:

$$\overline{\Delta\text{SoC}_m(t)} = \frac{1}{2} \frac{m^2}{N(N-1)} + \frac{1}{2} \frac{(N-1-m)^2}{N(N-1)} \quad (7)$$

Finally the value of the Q factor, i.e. the mean value over all cells, is

$$Q = \frac{1}{N} \frac{(2N-1)}{6} T_{ref} \quad (8)$$

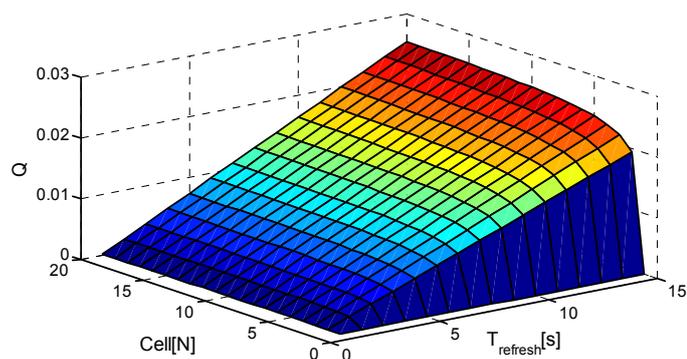


Figure 8: Quality factor Q versus number of cells (N) and refresh time (T_{ref}).

The Q value is directly proportional to the refresh time T_{ref} , i.e. an increase of the refresh time worsens the balancing effect. Moreover, increasing the number N of cells in the string worsens the balancing quality (even if not linearly). Figure 8 represents the trend of the quality factor Q as a function of cell number N and refresh time T_{ref} .

By using the realized prototype of BMS, i.e. a string of $N=7$ cells, the parameter Q has been experimentally calculated for different values of T_{ref} . Precisely, several values of Q have been measured with the same T_{ref} and different current profiles, and their mean value has been considered as final result. Measurements confirm the dependence of Q on T_{ref} , as Table 1 summarizes.

T_{ref} (s)	Q
2	$2.6 \cdot 10^{-4}$
5	$1.4 \cdot 10^{-3}$
10	$1.5 \cdot 10^{-3}$
20	$2.2 \cdot 10^{-3}$
30	$2.8 \cdot 10^{-3}$
60	$4.2 \cdot 10^{-3}$
90	$7.8 \cdot 10^{-3}$
120	$9.5 \cdot 10^{-3}$

Table 1: Experimentally measured Q factor (mean) for different values of refresh time T_{ref} .

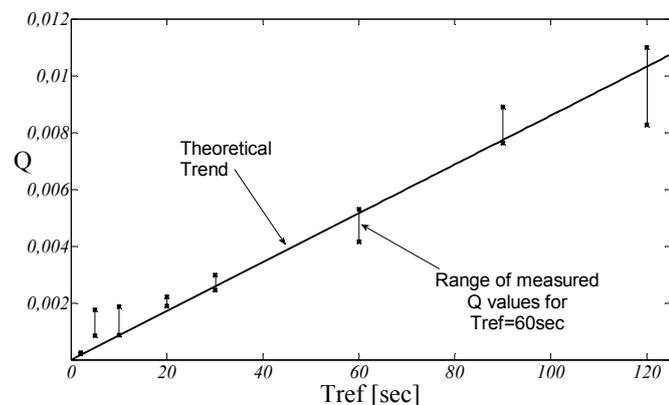


Figure 9: Theoretical Q factor values versus experimental Q measurements. Sets of measured Q values at the same refresh time are represented with vertical bars that define their range of variation, i.e. the experimental uncertainty.

Experimental results have been compared with Q values expected by (8) for $N=7$. Figure 9 compares calculated and

measured Q values. A good agreement is verified over all T_{ref} considered range, both in terms of trend and variance of measured data around expected values.

In order to visually highlight the balance worsening as T_{ref} increases, Figure 10 shows the comparison of the SoC of a 7-cell string in case of $T_{ref}=2s$ and $T_{ref}=120s$.

5. CONCLUSIONS

A new BMS for string-packs of Li-ion cells has been proposed. Core of the architecture is the technique of redundant cell, i.e. the reversible disconnection of a cell in the battery pack.

Main advantages of the proposed architecture are optimal balancing of the battery pack during operation and intrinsic hardness to cell faults. Moreover, the proposed architecture is very flexible, economical, stable and considerably space-saving.

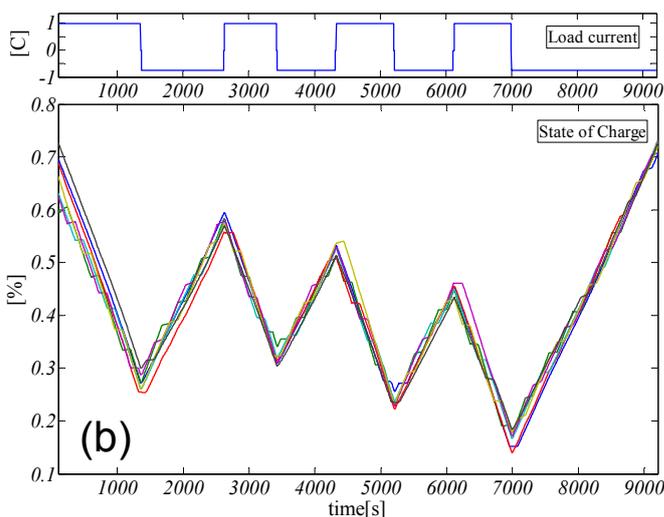
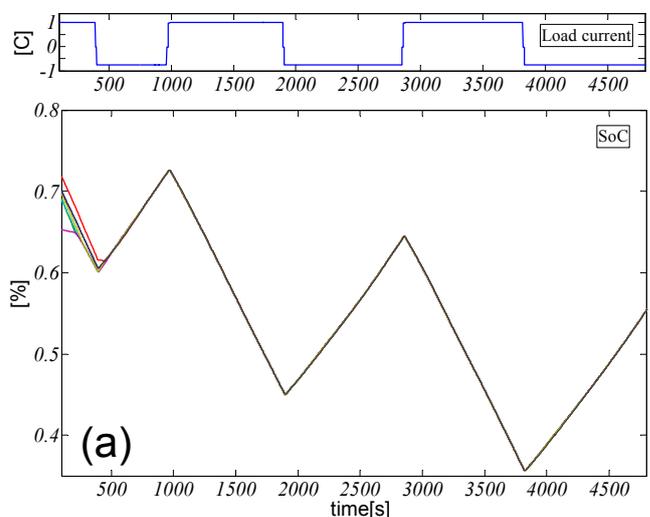


Figure 10: Comparison of the SoC of a 7-cell string in case of (a) $T_{ref}=2sec$ and (b) $T_{ref}=120sec$. The plot shows also the considered load current profile (each line represents one of the 7 cells).

A drawback is that a substantial effectiveness of the technique limits the dimension of the pack to about 10 cells, i.e. up to 500W. This means that the proposed BMS architecture is suited for low-power automotive applications,

such as electric scooters and bikes. For higher power demanding loads, a modular combination of several cell-redundant BMSs can be conceived. Of course, in this case the complexity of the layout also sensibly increases.

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