Σ-INTEGRATION ANALOG TO DIGITAL CONVERTER, IDEA, IMPLEMENTATION AND RESULTS

Pavel Píša * **Petr Porazil** **

* *Department of Control Engineering, Faculty of Electrical Engineering, Czech Technical University, Karlovo náměstí 13, 121 35 Praha 2, Czech Republic*
** *Osnice 37, 252 42 Jesenice, Czech Republic*

Abstract: The paper presents a new analog signal to digital representation conversion technique. The proposed approach tries to combine and preserve significant excellent features of double integration and sigma-delta analog to digital converters. The proposed AD-converter is constructed for a direct conversion of two analog signals ratio to the digital domain. The design uses an oversampling technique and the digital output resolution and bandwidth can be tuned by digital data post-processing. Other outstanding feature is an accurate area under signal curve measurement. The output data rate is constant (unlike for voltage-frequency converters) and the response time is maintained short without need of high modulator switching frequency. The described AD-converter features are a big advantage for the spectrophotometric absorbance measurement. Most of other measurement applications of AD-converters request mainly a great relative accuracy of conversion, but the absorbance is computed as a logarithm of the measured ratio between the measurement and the reference optical sensor response. The developed converter is already successfully used in serially produced UV-VIS spectrophotometric HPLC detectors. The converter has some drawback as well, the borders of sampling interval burden by some jitter although it has no influence on accumulated area computation.

Keywords: ADC, HPLC, detector, analog, converter, sigma-delta

1. INTRODUCTION

The paper presents a new analog signal to digital representation conversion technique. This technique has been invented in the new HPLC spectrophotometric detector design process. The analog to digital converter is one of the key components determining accuracy and sensitivity of HPLC detectors. The conversion of the analog signal before the digital logarithm and absorbance calculation is advantageous for higher stability better than for analog absorbance computation. This concept demands even higher converter stability and resolution. The evaluation of the required AD-converter properties can be found in (Píša and Porazil, 2003). The first part of the paper focuses on the ideas leading to the invention of the Σ-Integration conversion technique. An analysis of static and dynamic properties of the designed AD-converter and a brief overview of the electrical circuit realization are presented in the next parts of the paper. The last paragraphs demonstrate resolution and performance of the real serially produced instrument utilizing the described AD conversion technique.

2. DESIGN OF AD-CONVERTER WITH DEMANDED PARAMETERS

Because none of the standard AD-converter techniques has been considered to fully meet required parameters, the authors decided to develop an AD-converter optimized by its design for very high resolution ratio conversions. The authors already have an experience with the design of the AD-converters with double integration and usage of the sigma-delta AD-converters from former HPLC detectors projects. The new design is focused on the development of an AD-converter which would target to HPLC specific criteria. The usual AD-converter requirements are taken with lower priority.

The requested features are at least 22 bits uncorrelated samples at the frequency 1 Hz resolution, the conversion of ratio between the measurement and reference photodetector responses and the exact area under signal curve evaluation. The full in depth analysis is provided in (Píša and Porazil, 2003).

The sigma-delta modulator could be modified to continuously integrate the input signal in the form of the capacitor charge and the modulator could control the periodic subtraction of the quantized reference signal. A disadvantage of that approach is the necessity of a very high modulation frequency for strictly uncorrelated samples. The frequency of exactly uncorrelated samples at frequency 1 Hz and resolution 22 bits requires the modulation frequency of about 4.2 MHz or a higher order modulator. Higher order modulators results in unrealistic demand to used analog components if required stability has to be attained. The common sigma-delta AD-converters use the frequency of modulation of about 0.1 or 1 MHz. The high frequency of switching of the analog multiplexer for balancing by a reference signal would lead to increase of the noise. Each analog multiplexer switching leads to some small crosstalk of digital to analog signals. If the charge contributed by crosstalk is constant, it could be suppressed by some compensation. But the contributed noise would be a function of temperature, digital power voltage and other factors. This leads to the idea to use a converter with lower frequency of the primary modulator which needs to distinguish in order of magnitude more levels in each cycle than the conventional two level sigma-delta modulator.

The demand for the constant frequency of the modulator cycles and the continuous integration of the input signal can be achieved by initiating of the reference signal subtraction in periodic time points. The natural condition for the end of the reference signal application would be the time of zero-crossing of the integrator output. This setup would lead to a loss of exact (sub-clock) counting of the time quanta for the reference signal application. This means that the reaction to the zero-crossing needs to be delayed to the beginning of the next digital clock period. The remaining negative voltage value stored in the modulator integrator caused by the delayed comparison (seen as overshot) is automatically added to the input signal in the next modulator period. This enables to achieve a deterministic resolution enlargement when values from the modulator cycles are averaged. This enables to enhance resolution by oversampling and the exact area measurement. The frequency of the digital clock counting number of the applied reference quanta can be many times higher than the modulator frequency. The digital clock frequency is limited only by maximal frequency of the used digital counter. It makes 32 Mhz in the presented design and the value is limited only by the speed of the FPGA device used for the digital part of the AD-converter. The design can suppress even the influence of the voltage offsets, propagation delays and other limiting factors of the used components. The developed technique of the AD-converter consolidates advantages of the sigma-delta and integration AD-converters. The authors have labeled this technique as summation-integration, abbreviated as Σ-integration or Σ-$\int$ ADC. The proposed solution has some drawbacks as well and the AD-converter is not meant for general purposes. These disadvantages are pointed out at the end of the theoretical analysis bellow.

3. ANALYSIS OF Σ-INTEGRATION AD-CONVERTER

This paragraph describes the function and theoretically reachable parameters of the AD-converter built according to the previous considerations. The block diagram of the converter is shown in Figure 1. The conversion is realized by three main blocks. The digital clock generator ϕ_{clk} (period T_{clk}, frequency f_{clk}) synchronizes modulator periods ϕ_{mod} (period T_{mod}, frequency f_{mod}). The clock signal ϕ_{mod} is a result of the division of the digital clocks, $T_{mod} = T_{clk} \cdot L_{mod}$. Because all logic and digital processing of the AD-converter is synchronized by the clock signal ϕ_{clk}, the new symbol l is introduced to express the time intervals counted in the integer multiples of the period T_{clk}. The symbol L is used for periodic intervals (instead of l).

The first function block is a modulator (SumInt Analog Modulator). This modulator converts the ration of the analog input signals (measurement and reference) to a logic signal, which carries an information about the number of the applied

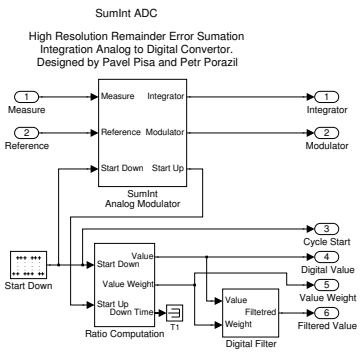

Fig. 1. Block Diagram of Σ-∫ AD-converter

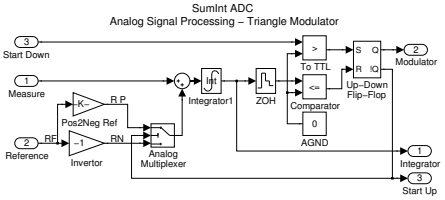

Fig. 2. Analog Part of Σ-∫ AD-converter

time quanta of the positive and negative reference signal (label Start Up). The application of the negative reference signal is controlled by a modulator clock signal (label Start-Down). The second block (Ratio Computation) computes the first stage digital output from the captured times of the previous signal changes (with T_{clk} resolution). Two digital values are computed, i.e. the ratio of the input signals (Value output) and the second auxiliary signal (Value Weight) described later. The last function block (Digital Filter) proceeds digital filtration of both output signals of the previous block and computes the converted digital value with final resolution. The described division into blocks is made according to the logical function of the blocks. Physical realization by analog circuits, FPGA device and controlling microcontroller is different.

3.1 Σ-Integration AD-converter Modulator

The detailed model of the analog part of the converter is shown in Figure 2. The basic block of the modulator is an analog integrator, which continuously integrates the measurement voltage input signal (u_m). The positive (RP, voltage u_{rp}) and negative (RN, voltage u_{rn}) reference signals are periodically switched by the analog multiplexer and the result is added to the integrator input. The ratio of positive to negative reference signals is selected by $K_{pos2neg}$ constant, which defines an input range of the AD-converter. Switching between two reference signals is provided by the analog multiplexer which is controlled by a flip-flop circuit. The integrator voltage output is compared with analog ground of the circuit. When

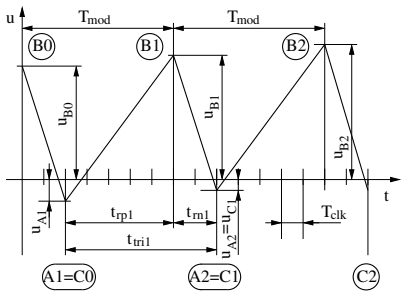

Fig. 3. Σ-∫ ADD Integrator Output

the integrator output crosses zero the multiplexer switches from RN to RP reference signal. The switching is not immediate, but is delayed to the next rising edge of the signal ϕ_{clk}. This leads to occurrence of small remaining negative voltage $u_{A\,i}$ on the integrator output at the time of the switch to signal RP. The multiplexer switches back to the signal RN at the beginning of the next modulator period defined by the clock signal ϕ_{mod}.

The resulting waveform of the integrator output has a triangle shape for the constant measurement and reference signals as shown in Figure 3. The rising course of the signal is defined by points A_i B_i for the cycle i of the modulator and the course time interval $t_{rp\,i} = l_{rp\,i} \cdot T_{clk}$ corresponds to the application of RP signal. The falling course B_i C_i corresponds to the RN signal application and takes time $t_{rn\,i} = l_{rn\,i} \cdot T_{clk}$. The both times are bounded by the condition $l_{pn\,i}, l_{rn\,i} \in \langle 0, L_{mod} \rangle$. The time of one triangular curve $t_{tri\,i}$ is given by the sum of both parts $t_{tri\,i} = t_{rp\,i} + t_{rn\,i}$. The timing of switching in points B_i is defined by the modulator period T_{mod} (l_{mod} cycles of ϕ_{clk}). This leads to the next equations for two consecutive curves B_{i-1} C_{i-1} and A_i B_i

$$t_{rp\,i} = T_{mod} - t_{rn\,i-1} \tag{1}$$

$$l_{rp\,i} = L_{mod} - l_{rn\,i-1} \tag{2}$$

The integrator output voltage u is defined by the next expressions

$$u_{A\,i} = u_{C\,i-1} \tag{3}$$

$$\Delta u_{AB\,i} = \int_{t_{A\,i}}^{t_{B\,i}} (u_m(t) + u_{rp})\ dt \tag{4}$$

$$\Delta u_{BC\,i} = \int_{t_{B\,i}}^{t_{C\,i}} (u_m(t) + u_{rn})\ dt \tag{5}$$

These equations expect a quasi-static value of the reference voltage and arbitrarily variable value of the measurement input voltage u_m. The input frequency range should be limited by a filter for the real integrator device to suppress non-symmetric influence of noise to the integrator output. The next expression describes a change

of the remainder integrator output voltage over a triangle course.

$$\Delta u_{AC\,i} = \Delta u_{AB\,i} + \Delta u_{BC\,i} \tag{6}$$

The integral of the measured signal u_m can be substituted by its mean value $\overline{u_{m\,i}}$ for cycle i. The equations (4), (5) can be rewritten as

$$\begin{aligned}
\Delta u_{AC\,i} &= u_{rp} t_{rp\,i} + u_{rn} t_{rn\,i} + \int_{t_{B\,i}}^{t_{C\,i}} u_m(t)\,dt \\
\Delta u_{AC\,i} &= u_{rp} t_{rp\,i} + u_{rn} t_{rn\,i} + \overline{u_{m\,i}}\, t_{tri\,i} \\
\Delta u_{AC\,i} &= T_{clk}\ (u_{rp} l_{rp\,i} + u_{rn} l_{rn\,i} \cdots \\
&\quad + \overline{u_{m\,i}}\ (l_{rp\,i} + l_{rn\,i}))
\end{aligned} \tag{7}$$

These equations are similar to the equations of the AD-converter with double integration for the hypothetical presumption $\Delta u_{AC\,i} = 0$. It is possible to compute the mean value of the input signal from one triangular curve

$$\overline{u_{m\,i}} = -\frac{u_{rp} l_{rp\,i} + u_{rn} l_{rn\,i}}{l_{rp\,i} + l_{rn\,i}} + \frac{\Delta u_{AC\,i}}{T_{clk}\,(l_{rp\,i} + l_{rn\,i})} \tag{8}$$

One cycle conversion leads to a theoretical resolution with $l_{rp\,i} + l_{rn\,i} = l_{tri\,i}$ distinguishable levels. The error caused by the nonzero value of $\Delta u_{AC\,i}$ should be added to the considerations. Two worst cases could be considered

- $u_{A\,i}$ reaches its maximal negative value and $u_{C\,i} = u_{A\,i+1} = 0$
- the inverse case occurs for $u_{A\,i} = 0$ and $u_{C\,i} = u_{A\,i+1}$ with maximal negative value

The maximal negative remainder value $u_{A\,i}$ appears when zero crossing occurs exactly after the beginning of the T_{clk} period and value of u_m is minimal over this T_{clk} period. Because the application expects conversion of the signals given by light sensors, only positive signals need to be considered and minimum is equivalent to the input $u_m = 0$. Minimum of the remainder $u_{A\,i}$ is given by integration of the negative reference RN over period T_{clk}. The next bounding ranges for value $u_{A\,i}$ and conversion error can be computed as

$$\begin{aligned}
u_{A\,i} &\in \langle u_{rn}\, T_{clk}, 0 \rangle \\
\left| \frac{\Delta u_{AC\,i}}{T_{clk}\,(l_{rp\,i} + l_{rn\,i})} \right| &\le \frac{-u_{rn}}{l_{rp\,i} + l_{rn\,i}}
\end{aligned} \tag{9}$$

The real resolution of one triangle curve cannot be computed because the value $l_{tri\,i} = l_{rp\,i} + l_{rn\,i}$ is not constant (it depends on previous curve). The average values are bound by modulator synchronization in points B_i with a constant period, $\overline{l_{tri\,i}} = L_{mod}$ ($\overline{t_{tri\,i}} = T_{mod}$). The variations are not so big for the steady state. But the converter is not designed for one modulator cycle conversion. The design enables measurement of the mean value over more up-to infinite cycles on contrary. The resolution is expected to linearly increase and to be limited only by parameters of the used components.

The next equations describe measurement of the mean value over n triangular curves $(i, \ldots, i+n-1)$ from equation (7) describing one curve case and modulator switching rules (2) and (3).

$$\begin{aligned}
\Delta u_{A\,i\,A\,i+n} &= T_{clk} \sum_{j=0}^{n-1} (u_{rp} l_{rp\,i+j} + u_{rn} l_{rn\,i+j} \\
&\quad + \overline{u_{m\,i+j}}\ (l_{rp\,i+j} + l_{rn\,i+j})) \\
\frac{\Delta u_{A\,i\,A\,i+n}}{T_{clk}} &= u_{rp} \sum_{j=0}^{n-1} l_{rp\,i+j} + u_{rn} \sum_{j=0}^{n-1} l_{rn\,i+j} \cdots \\
&\quad + \overline{u_{m\,i,n}}\ (n\, L_{mod} + l_{rp\,i} - l_{rp\,i+n})
\end{aligned}$$

The mean value $\overline{u_{m\,i,n}}$ on the interval $(i, \ldots, i+n-1)$ can be simply evaluated. The maximal error can be evaluated from the maximal possible difference of the remainders $u_{A\,i}$ at the beginning and $u_{A\,i+n}$ at the end of the measurement interval. This contribution to error is labeled $u_{aaerr\,i,n}$ and is equivalent to equation (9) for one curve conversion

$$\begin{aligned}
\overline{u_{m\,i,n}} &= -\frac{u_{rp} \sum_{j=0}^{n-1} l_{rp\,i+j} + u_{rn} \sum_{j=0}^{n-1} l_{rn\,i+j}}{n\, L_{mod} + l_{rp\,i} - l_{rp\,i+n}} \cdots \\
&\quad + u_{aaerr\,i,n}
\end{aligned} \tag{10}$$

$$|u_{aaerr\,i,n}| \le \frac{-u_{rn}}{n\, L_{mod} + l_{rp\,i} - l_{rp\,i+n}} \tag{11}$$

It is possible to compute real converter minimal resolution for case of measurement over n cycles of the modulator which is equal to $(n-2)\, L_{mod}$ for $l_{pn\,i}, l_{rn\,i} \in \langle 0, L_{mod} \rangle$. This result is only theoretical because of necessity to limit the input range to a stable region of the modulator operation as described in the next paragraphs. The error given by $u_{aaerr\,i,n}$ is smaller than one distinguishable level. The number of transfered and processed digital values can be decreased by some substitutions in the equation (10). The next substitutions are considered

$$\begin{aligned}
\sum_{j=0}^{n-1} l_{rn\,i+j} &= l_{rn\,i,n} \\
\sum_{j=0}^{n-1} l_{tri\,i+j} &= n\, L_{mod} + l_{rp\,i} - l_{rp\,i+n} = l_{tri\,i,n} \\
\sum_{j=0}^{n-1} l_{rp\,i+j} &= l_{tri\,i,n} - l_{rn\,i,n}
\end{aligned}$$

The equation (10) can be transformed into the next form

$$\overline{u_{m\,i,n}} = -\frac{u_{rp}\,(l_{tri\,i,n} - l_{rn\,i,n}) + u_{rn}\,l_{rn\,i,n}}{l_{tri\,i,n}} \cdots$$
$$+u_{aaerr\,i,n}$$
$$\overline{u_{m\,i,n}} = -u_{rp} + \frac{l_{rn\,i,n}}{l_{tri\,i,n}}\,(-u_{rn} - u_{rp}) \cdots$$
$$+u_{aaerr\,i,n} \tag{12}$$

3.2 Stability of Σ-Integration Modulator

Stability of the designed modulator must be checked, because one cycle contributes to following cycles by an initial remainder voltage and variable rising course start time. This problem is not obvious from the previous considerations.

The effect of the remainder is negligible. The full prove can be found in (Píša and Porazil, 2003). The most important result of the analysis is development of value $u_{B\,i}$ in time. If a deviations $\widetilde{u_{B\,i}}$ to the final steady value of $u_{B\,i}$ decrease, the conversion process is stable.

$$\widetilde{u_{B\,i+1}} = \frac{u_m + u_{rp}}{u_m + u_{rn}}\widetilde{u_{B\,i}} \tag{13}$$

The stability region is bounded by a condition of the deviation $\widetilde{u_{B\,i}}$ amplification in the range $(-1, 1)$ which leads to the next inequalities

$$\left|\frac{u_m + u_{rp}}{u_m + u_{rn}}\right| < 1 \tag{14}$$
$$|u_m + u_{rp}| < |u_m + u_{rn}|$$

The before considered conditions $u_m < -u_{rn}$ and $u_m > -u_{rp}$ ensure that the fraction numerator is always positive and the fraction denominator is always negative. Then the conditions can be rewritten into the form

$$u_m + u_{rp} < -u_m - u_{rn}$$
$$u_m < \frac{1}{2}\,(-u_{rn} - u_{rp})$$

The usable input signal u_m range for stable modulator operation can be determined taking all the above derived conditions

$$u_m \in \left(-u_{rp},\ \frac{1}{2}\,(-u_{rn} - u_{rp})\right) \tag{15}$$

The above proven analysis leads to the conclusion that only one half of the initially considered input range can be utilized. This condition is not too restrictive because the actual input range can be arbitrarily adjusted by modification of the multiplication factors in the reference signals RN and RP amplifiers. The input range limitation influences only the theoretical resolution of the converter.

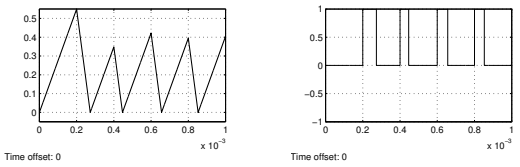

Fig. 4. Simulated Signal Curves of Σ-∫ Modulator

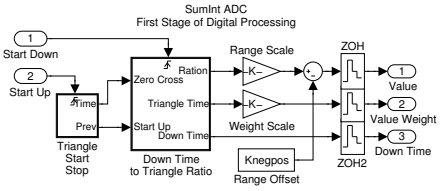

Fig. 5. The First Digital Stage of Σ-∫ AD-converter

The resolution can be finally determined from the equations (9) and (11) but the range of the values $l_{rn\,i}$ is restricted to an interval $\langle 0,\ \frac{1}{2}L_{mod}\rangle$ and the range of the value $l_{pn\,i}$ is restricted to a range $\langle \frac{1}{2}L_{mod},\ L_{mod}\rangle$. This leads to a decrease of the primarily distinguishable levels of the modulator to $\frac{1}{2}L_{mod}$. The range of difference $l_{rp\,i} - l_{rp\,i+1}$ is decreased twice as well. This leads to a final resolution equation for the Σ-Integration AD-converter n modulation cycles conversion with the period T_{mod} (L_{mod})

$$(n-1)\,\frac{1}{2}L_{mod} \tag{16}$$

A typical curve of the modulator integrator output of the Σ-Integration AD-converter is shown in Figure 4. These curves were produced by a model created in the **Simulink** environment. The stabilization of the vertex value $u_{B\,i}$ is well visible in this figure.

3.3 Digital Processing of Σ-∫ Modulator Output

Digital processing of the modulator output is a little more complicated than for traditional sigma-delta AD-converters because the conversion time is not strictly constant. The best results are obtained when both signals carrying information from the modulator (triangle time $l_{tri\,i}$ and negative reference application time $l_{rn\,i}$) are filtered separately and the resulting ratio is computed after all other signal processing procedures.

Many methods of the FIR filter design can be used the same way as for conventional sigma-delta AD-converts. Convolution with usual $sinc(x)$ function can be used. The other possible filter type is a convolution with a Gaussian profile which would lead to smaller distortion of HPLC peak profiles which are the same or similar in shape to Gaussian profiles. Even simple or double moving average gives suitable results.

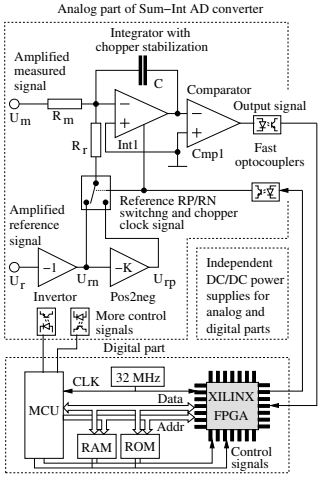

Fig. 6. The Electronic Implementation Block Diagram

4. CIRCUIT REALIZATION OF Σ-∫ AD-CONVERTER

The modulator logic has been realized in XILING FPGA circuit. The decimator has been inbuilt into FPGA as well. The SRAM FPGA is programmed by a microcontroller after power-on. The microcontroller contributes to an additional signal processing, logarithm computation, monochromator and light source control, communication with PC software and local user interface. A simplified block diagram of the Σ-Integration AD-converter electronics is presented in Figure 6.

The most important component of the AD-converter is the analog part of the modulator and amplification of very low current output signals of the diode photodetectors. The heart of the modulator is an integrator operational amplifier. A precious chopper-stabilized amplifier has been selected. The chopper-stabilization of the input voltage offset is even synchronized with the modulator period clock ϕ_{mod} to eliminate the undesirable aliasing of the chopper-stabilization with modulator periods. A high grade analog multiplexer has been used for the reference signal switching because leakage currents in the multiplexer could lead to deviations. An advantage of the design is that the parameters of the most other components are not critical. The invariability and low value of the comparator propagation delay are not required by our AD-converter design. Even the comparison level of the comparator does not need to be stable. The propagation delay of two high-speed optocouplers (20 MBd) for the comparator output and analog multiplexer control is suppressed by the design. Only jitter of the optocoupler for the multiplexer control signal contributes to the deviation of the AD-converter.

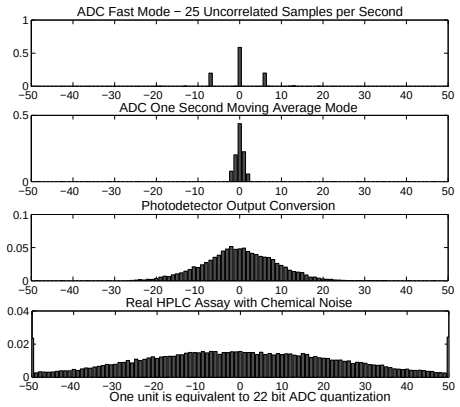

Fig. 7. The code distribution histogram for constant input signal

5. MEASURED RESULTS

The results has been obtained on **XILINX FPGA** ADC implementation of converter used in **LCD5000** spectrophotometers. The 32 MHz clock signal ϕ_{clk} is used for the control logic. The modulator periods and triangle curves are synchronized by the 5 kHz signal ϕ_{mod}.

The histograms of conversion output codes distribution for the DC input signal is shown in Figure 7. The fast mode is equivalent to 25 Hz 19-bit conversion, that is why the output codes are located at the isolated values. When moving average filtering length is set to one second, theoretical resolution increases up to 24-bits. That is more than the demonstrated 22-bit histogram resolution, but the theoretical single code distribution is widened by noise. The AD-converter contributes many times lower noise than the used photodetector or even HPLC assay chemical background.

6. CONCLUSION

The described Σ-∫ AD-converter was designed and successfully tested by authors as a part of their work for PiKRON Ltd. company regarding the project concerning a new generation of the liquid chromatography spectrophotometric detector LCD5000. The detectors have already been produced and used by various European universities and institutions and the developed solution proved to be very stable and noise suppressing. Authors were allowed by PiKRON Ltd to publish the company development results because this solution can attract more areas than HPLC systems.

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