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THE EMBEDDED VISION SYSTEM FOR PORTABLE APPLICATIONS

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Abstract: A simple and cost-effective time switching method is to connect two camera modules into one camera interface port. The suggested embedded vision system is implemented and the image taken as expected. The design requirements for the hardware and the device driver are also considered. The captured image quality proves our suggestion could be a good candidate for two camera interface solutions without using complicated DSPs or FPGAs. *Copyright © 2008 IFAC*

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1. Introduction

Embedded systems with camera interfaces are steadily growing up due to increasing demand in areas such as mobile phone, mobile multimedia player, digital camera, and so on. The purpose of such systems is currently not only to acquire images, to be viewed or analyzed but also to process these images automatically, in order to extract useful information and execute tasks of different complexities. To perform embedded image processing, electronic vision systems require a wide variety of devices such as micro-controllers, micro-processors, DSPs, and reconfigurable structure like FPGAs(Field Programmable Gate Array) [Fabio et al, and Mathias]. These systems have a number of common constraints: low cost, low power, limited amount of on-board memory, and real time operation.

In some specific cases requiring two or more camera interfaces, the camera interfacing method like Fig. 1 using DSPs and FPGAs is not an attractive way due to the design complexity. To attack this problem, we introduced a time switching method like Fig. 2 which is simple and cost-effective. In this paper, we implemented time switching vision port for two camera interfaces.

2. System design

We'd developed an embedded system with a single camera module which is shown in Figure 3. We used the S3C2440A by SAMSUNG as the main CPU and Windows CE 5.00 as the operating system. The main CPU has a specialized port for camera interface. In most cases requiring one camera module, the port is very effective to interconnecting the camera module and the main CPU. However, some embedded systems need two or more camera interfaces. Those cases, mostly adopting the direct-hardware control method using microprocessors, DSPs, FPGAs, and etc, make the system design tedious and complicated. So, we try to give a simple solution to implement two-camera adopting the simple timing-switching method. The suggested embedded system for two camera ports is almost the same as the embedded system shown in Fig. 3 except for the number of the camera module.
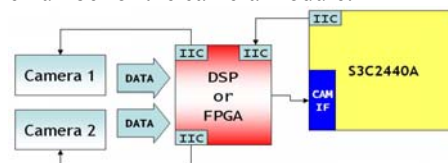

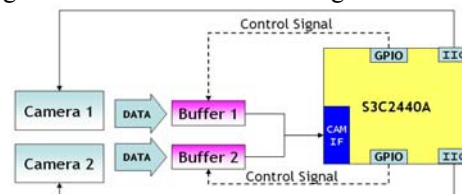
Fig. 1 Conventional method using DSP or FPGA

Fig. 2 Proposed method

Fig. 3 Embedded system with single camera module

3. Implementation

Our camera modules contain an Omnivision OV9653 sensor and an integrated lens. The OV9653 contains a 1280X1024 color CMOS camera array. It uses the Serial Camera Control Bus, SCCB (IIC for intents and purposes) interface for control. Fig. 4 is the functional block diagram of the OV9653. The chip is controlled modifying the registers through the SSCB interface by SIO_C and SIO_D in Fig. 4

[Thorsen and Ommivison 2005, 2003]. XVCLK1 driven by the camera processor is connected to the CAMCLK of the main CPU, S3C2440A as the system clock input. PCLK also driven by camera processor is connected to the CAMPCLK as the camera clock reference of the main CPU like Fig. 5.

The camera interface in the S3C2440A supports the YCbCr 4:2:0 or 4:2:2 image data and the RGB 16/24-bit image data[SAMSUNG Elec.]. For the noise reduction, the camera interface IOs were to be Schmitt-trigger type IOs. In our design, we inserted the 74LVC244A, which is the non inverting buffer/line driver with 3-state outputs between the camera and the main CPU.
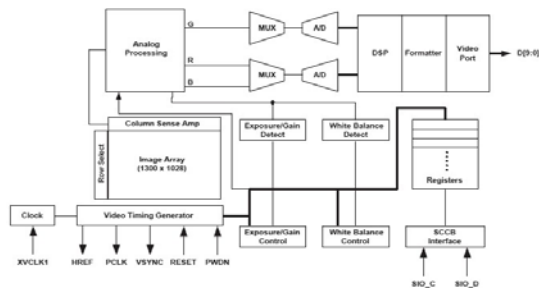

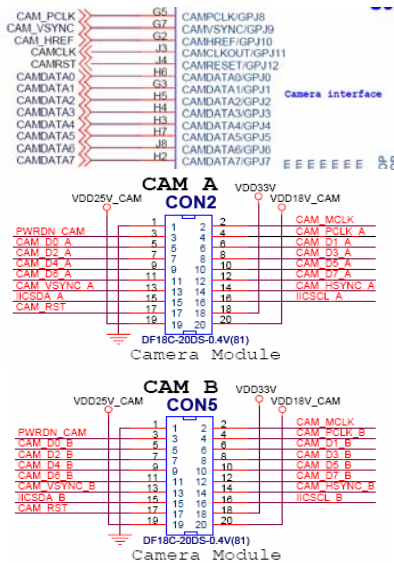Fig. 4 Functional block diagram

Fig. 5 Circuit of camera interfaces

As shown in Fig. 5, the data bus of camera A and B were mapped to the specialized camera interface port commonly. We assigned the IIC signal set, SSCB to the different IIC channel of the main CPU to initialize and control the camera module independently. We turned off the buffer connected to CAM_B to accept the image data only from CAM_A and vice versa. In our design, the time delay for the command signal is inevitable for each image transfer step. It's primarily because the CPU can't send the control signal to two camera modules coincidently. Therefore, the timing control of receiving the image data from camera modules needs to be carefully handled. Furthermore, the fact that the device driver

on operating system, here WinCE, can't control the device in a real time, makes the system design more difficult and complex. We modified the parameters from various locations such as the variables in the device driver, board routing lengths and paths in hardware to optimize the system with two camera interfaces.

4. Results

Fig. 6 shows the embedded system with two camera interfaces and Fig. 7 is the image captured from test application. In the system, the image can be received separately from each camera and reconstructed into one image. The mixed image from the file systems of OS is saved as a bmp file. The captured image quality proves our suggestion could be a good candidate for two camera interface solutions without using complicated DSPs or FPGAs.
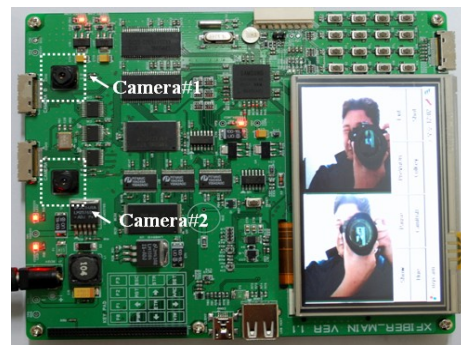

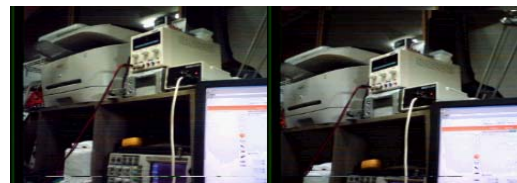Fig. 6 Embedded system with two camera interfaces

Fig. 7 Image from the suggested embedded system

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